M.2 2280 PCIe/NVMe SSD 720-C Datasheet

(SQF-C8Bxx-xxxGCEDC) (B+M Key)

CONTENTS

Revision History

Rev.	Date	History
1.0	2021/3/3	1. Premilitary
1.1	2021/4/20	1. Add Hardware Write Protect Pin information

1. Overview

Advantech SQFlash 720-C series M.2 2280 (B+M Key) PCIe/NVMe SSD (Solid State Drive) delivers all the advantages of flash disk technology with PCIe Gen3 x2 interface and is fully compliant with the standard Next Generation Form Factor (NGFF) called M.2 Card Format. SQF-C8B M.2 2280 offers up to 2048GB and its performance can reach up to 1700 MB/s read and 1500 MB/s write based on Kioxia 3D TLC flash. Moreover, the power consumption of SQF-C8B M.2 2280 is much lower than traditional hard drives, making it the best embedded solution for new platforms.

2. Features

- **PCIe Interface**
  - Compliant with NVMe 1.3
  - PCI Express Base 3.1
  - PCIe Gen 3 x 2 lane & backward compatible to PCIe Gen 2 and Gen 1
  - Support up to QD 128 with queue depth of up to 64K
  - Support power management (optional)
- **Operating Voltage：3.3V**
- **Support LDPC of ECC algorithm**
- **Support SMART and TRIM commands**
- **Temperature Ranges[1]**
  - Commercial Temperature
    - 0℃ to 70℃ for operating
    - -40℃ to 85℃ for storage

  *Note : 1. Based on SMART Attribute (Byte index [2 :1] of PCIe-SIG standard, which measured by thermal sensor
- **Mechanical Specification**
  - Shock：1,500G / 0.5ms
  - Vibration：20G / 80~2,000Hz
- **Humidty**
  - Humidity：5% ~ 95% under 55℃
- **Acquired RoHS、WHQL、CE、FCC Certificate**
- **Acoustic：0 dB**
- **Dimension：80.0 mm x 22.0 mm x 3.8 mm**

3. Specification Table

■ Performance

* Preliminary, subject to change based on firmware migration.

		Sequential Performance (MB/sec)		Random Performance (IOPS @4K)	
		Read	Write	Read	Write
3D TLC (BiCS4)	128 GB	1,500	500	70K	100K
	256 GB	1,700	1,000	140K	200K
	512 GB	1,700	1,400	200K	300K
	1 TB	1,700	1,480	200K	320K
	2 TB	1,700	1,350	150K	300K

NOTES:

1. The performance was estimated based on Toshiba 3D TLC BICS4 flash.
2. Performance may differ according to flash configuration and platform.
3. The table above is for reference only. The criteria for MP (mass production) and for accepting goods shall be discussed based on different flash configuration

Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a SSD can be written which is a measurement of SSDs' expected lifespan, represents the amount of data written to the device.

TBW = [(NAND Endurance) x (SSD Capacity)] / WAF

- **NAND Endurance**: Program / Erase cycle of a NAND flash.
  - SLC: 100,000 cycles
  - Ultra MLC: 30,000 cycles
  - MLC: 3,000 cycles
  - 3D TLC (BiCS3/BiCS4): 3,000 cycles
- **SSD Capacity**: SSD physical capacity in total of a SSD.
- **WAF**: Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

WAF = (Lifetime write to flash) / (Lifetime write to host)

Endurance measurement is based on JEDEC 219A client workload and verified with following workload conditions,

- PreCond%full = 100%
- Trim commands enabled
- Random data pattern.

- **SQFlash 720-C M.2 2280 TBW**

	WAF	TBW
		3D TLC (BiCS4)
128 GB	3.5	110
256 GB	3.2	240
512 GB	2.9	520
1 TB	2.7	1120
2 TB	2.5	2400

4. General Description

Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, SQF-C8B 720-C applies the LDPC algorithm, which can detect and correct data errors even with the latest 3D TLC technology to ensure data being read correctly, and protects data from corruption.

Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, when flash media is not used evenly, some blocks get updated more frequently than others and the lifetime of device would be reduced significantly. Thus, wear leveling is applied to extend the lifespan of NAND flash by evenly distributing write and erase cycles across the media.

SQFlash 720-C series provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static wear leveling algorithms, the life expectancy of the NAND flash is greatly improved.

Bad Block Management

Bad blocks are blocks that do not function properly or contain more invalid bits causing stored data unstable, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Early Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. SQFlash 720-C series implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages bad blocks that appear with use. This practice prevents data being stored into bad blocks and further improves the data reliability.

Power Loss Protection: Flush Manager

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, SQFlash SSD applies the Flush Manager technology, only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

In addition, it is critical for a controller to shorten the time the in-flight data stays in the controller internal cache. Thus, SQFlash applies an algorithm to reduce the amount of data resides in the cache to provide a better performance. With Flush Manager, incoming data would only have a “pit stop” in the cache and then move to NAND flash directly. Also, the onboard DDR will be treated as an “organizer” to consolidate incoming data into groups before written into the flash to improve write amplification.

TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD so that blocks of data that are no longer in use can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks at all time.

SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a solid state drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users impending failures while there is still time to perform proactive actions, such as save data to another device.

Over-Provision

Over Provisioning refers to the preserving additional area beyond user capacity in a SSD, which is not visible to users and cannot be used by them. However, it allows a SSD controller to utilize additional space for better performance and WAF. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

Thermal Throttling

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. Thermal Throttling function is for protecting the drive and reducing the possibity of read / write error due to overheat. The temperature is monitored by the thermal sensor. As the operating temperature continues to increase to theshold temperature, the Thermal Throttling mechanism is activated. At this time, the performance of the drive will be significantly decreased to avoid continuous heating. When the operating temperature falls below theshold temperutue, the drive can resume to normal operation.

Advanced Device Security Features

- Advanced Encryption Standard (AES)

  An AES 256-bit encryption key is generated in the drive's security controller before the data gets stored on the NAND flash. When the controller or firmware fails, the data that is securely stored in the encryption key becomes inaccessible through the NAND flash.

- Secure Erase

  SQFlash 720-C series supports standard NVMe command secure erase. Also, with internal AES encryption support, the erase process will start with resetting AES key. By doing so, existing data will be scrumbled within 10ms and cannot be recovered anymore. Moreover, erase flag is set when erase function is triggered, which will ensure the whole erase process can be 100% completed. Even there's power interrupt, after power resume, erase operation will be resume right away as well.

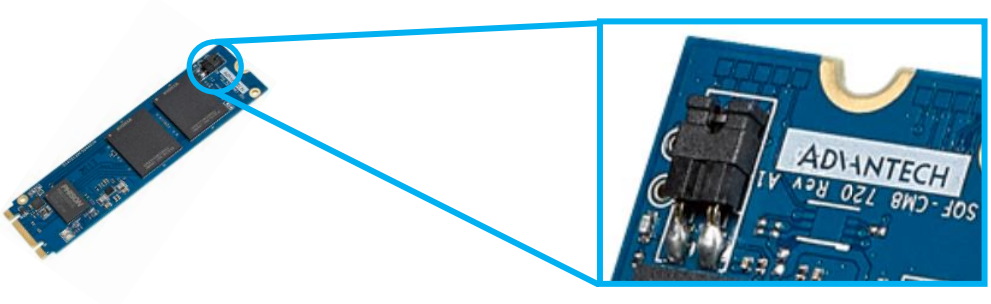
- OPAL 2.0 support

  SQFlash 720-C series supports standard OPAL 2.0 function for advance Self-Encryption Drive (SED) feature sets. Advantech provides also user friendly interface for setting disk / system bonding to prevent SSD be used in non-authorized platforms, which is called Flash Lock function.

- Hardware Write Protect Pin

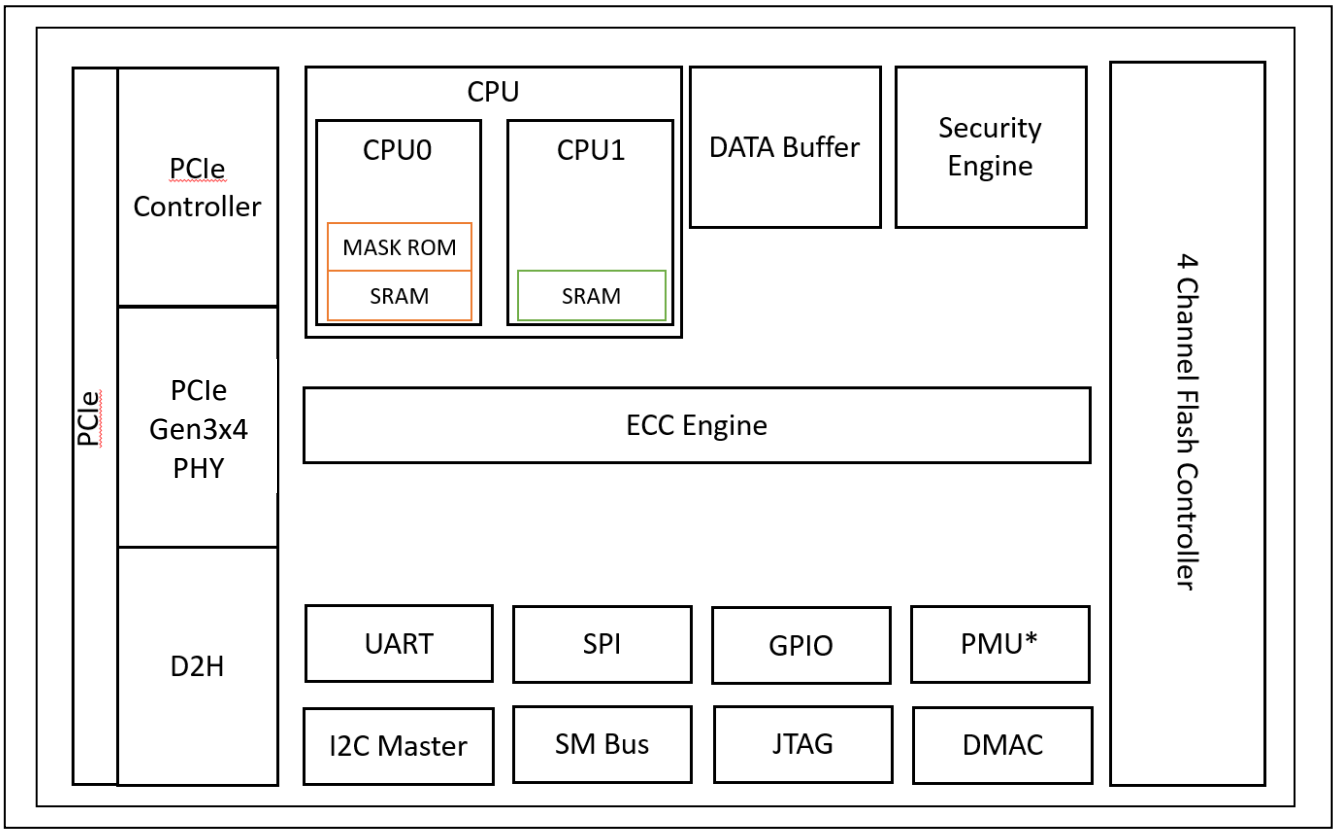
  A 2-pin header is mounted and connected to controller reserved GPIO for the drive write protection. When the pins are opened, all of the write command will be carried to a buffer area without real programming to the Flash IC. So the data won't be saved in this mode and will be totally discarded upon power shutting down.

  GPIO pin is reserved on the PCB without any default function. Optionally the pin can be set to Write Protect by loading the specific version firmware. Please contact Advantech sales representative if you would like to enable the function.



On-board GPIO for Write Protection

Block Diagram



■ LBA value

Density	LBA
128 GB	250,069,680
256 GB	500,118,192
512 GB	1,000,215,216
1 TB	2,000,409,264
2 TB	4,000,797,360

5. Pin Assignment and Description

Below table defines the signal assignment of the internal NGFF connector for SSD usage, described in the PCI Express M.2 Specification version 1.1 of the PCI-SIG.

Pin No.	PCIe Pin	Description
1	GND	CONFIG_3 = Ground
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	N/C	No connect
6	N/C	No connect
7	N/C	No connect
8	N/C	No connect
9	N/C	No connect
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	N/C	No connect
12	Module Key B	Module Key
13	Module Key B	
14	Module Key B	
15	Module Key B	
16	Module Key B	
17	Module Key B	
18	Module Key B	
19	Module Key B	
20	N/C	No connect
21	GND	Ground
22	N/C	No connect
23	N/C	No connect
24	N/C	No connect
25	N/C	No connect
26	GPIO_WP	Write Protection GPIO (optional)
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	N/C	No connect
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform (Reserve)
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pull-up on platform (Reserve)

43	PETp0	PCIe TX Differential signal defined by the PCIe 3.0 specification
44	ALERT#(O) (0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active low
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Substates.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	GPIO_QE	Quick Erase GPIO (optional)
68	SUSCLK(32KHz) (I/O)(0/3.3V)	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module.
69	NC	CONFIG_1 = No connect
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	CONFIG_2 = Ground

6. NVMe Command List

■ Admin commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
0Dh	Namespace Management
10h	Firmware Activate
11h	Firmware Image Download
14h	Device Self-test
15h	Namespace Attachment
18h	Keep Alive
NVM Command Set Specific	
80h	Format NVM
81h	Security Send
82h	Security Receive
84h	Sanitize

■ NVM commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

7. Identify Device Data

The Identity Device Data enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero

■ Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	SN
63:24	M	Model Number (MN)	Model Number
71:64	M	Firmware Revision (FR)	FW Name
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M	IEEE OUI Identifier (IEEE)	Assigned by IEEE/RAC
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x09
79:78	M	Controller ID (CNTLID)	0x0000
83:80	M	Version (VER)	0x00010300
87:84	M	RTD3 Resume Latency (RTD3R)	0x124F80
91:88	M	RTD3 Entry Latency (RTD3E)	0x2191C0
95:92	M	Optional Asynchronous Events Supported (OAES)	0x00000100
99:96	M	Controller Attributes (CTRATT)	0x00000000
111:100	-	Reserved	0x00
127:112	O	FRU Globally Unique Identifier (FGUID)	0x00
239:128	-	Reserved	0x00
255:240	-	Refer to the NVMe Management Interface Specification for definition	0
257:256	M	Optional Admin Command Support (OACS)	0x001F
258	M	Abort Command Limit (ACL)	0x00
259	M	Asynchronous Event Request Limit (AERL)	0x03
260	M	Firmware Updates (FRMW)	0x12
261	M	Log Page Attributes (LPA)	0x0E
262	M	Error Log Page Entries (ELPE)	0x0F
263	M	Number of Power States Support (NPSS)	0x04
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes	0x01

		(APSTA)	
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x155
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x157
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x2710
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x00000000(HMB off)Depend on Disk Size(HMB on)
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x00000000(HMB off)Depend on Disk Size(HMB on)
295:280	O	Total NVM Capacity (TNVMCAP)	non-zero
311:296	O	Unallocated NVM Capacity (UNVMCAP)	0
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00000000
317:316	O	Extended Device Self-test Time (EDSTT)	0x001E
318	O	Device Self-test Options (DSTO)	0x01
319	M	Firmware Update Granularity (FWUG)	0x4
321:320	M	Keep Alive Support (KAS)	0x0001
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	1
325:324	O	Minimum Thermal Management Temperature (MNTMT)	0x111
327:326	O	Maximum Thermal Management Temperature (MXTMT)	0x157
331:328	O	Sanitize Capabilities (SANICAP)	0x00000006
511:316	-	Reserved	0
NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	M	Maximum Outstanding Commands (MAXCMD)	0
519:516	M	Number of Namespaces (NN)	0x000000001
521:520	M	Optional NVM Command Support (ONCS)	0x005F
523:522	M	Fused Operation Support (FUSES)	0
524	M	Format NVM Attributes (FNA)	0x01
525	M	Volatile Write Cache (VWC)	0x01
527:526	M	Atomic Write Unit Normal	0x00FF

		(AWUN)	
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x0000
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Reserved	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0000
535:534	M	Reserved	0x0000
539:536	O	SGL Support (SGLS)	0x0000000000
767:540	M	Reserved	0x00
IO Command Set Attributes			
2047:704	M	Reserved	0
2079:2048	M	Power State 0 Descriptor	0x0081031600401C52000000000000025800000258000003 16
2111:2080	O	Power State 1 Descriptor	0x0081031600401C52010101010000025800000258000003 16
2143:2112	O	Power State 2 Descriptor	0x0081031600401C52020202020000025800000258000003 16
2175:2144	O	Power State 3 Descriptor	0x0081031600401C5203030303000003E8000003E8030003E8
2207:2176	O	Power State 4 Descriptor	0x0081031600401C5224040404000186A00000138803000032
…	-	(N/A)	0
3071:3040	O	Power State 31 Descriptor	0
Vendor Specific			
4095:3072	O	Vendor Specific (VS)	Vendor Reserved

■ Identify Namespace Data Structure & NVM Command Set Specific

Bytes	Description
7:0	Namespace Size (NSZE)
15:8	Namespace Capacity (NCAP)
23:16	Namespace Utilization (NUSE)
24	Namespace Features (NSFEAT)
25	Number of LBA Formats (NLBAF)
26	Formatted LBA Size (FLBAS)
27	Metadata Capabilities (MC)
28	End-to-end Data Protection Capabilities (DPC)
29	End-to-end Data Protection Type Settings (DPS)
30	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)
31	Reservation Capabilities (RESCAP)
32	Format Progress Indicator (FPI)
33	Deallocate Logical Block Features (DLFEAT)
35:34	Namespace Atomic Write Unit Normal (NAWUN)
37:36	Namespace Atomic Write Unit Power Fail (NAWUPF)
39:38	Namespace Atomic Compare & Write Unit (NAWWU)
41:40	Namespace Atomic Boundary Size Normal (NABSN)
43:42	Namespace Atomic Boundary Offset (NABO)
45:44	Namespace Atomic Boundary Size Power Fail (NABSPF)
47:46	Namespace Atomic Optimal IO Boundary (NOIOB)
63:48	NVM Capacity (NVMCAP)
103:64	Reserved
119:104	Namespace Globally Unique Identifier (NGUID)
127:120	IEEE Extended Unique Identifier (EUI64)
131:128	LBA Format 0 Support (LBAF0)
135:132	LBA Format 1 Support (LBAF1)
139:136	LBA Format 2 Support (LBAF2)
143:140	LBA Format 3 Support (LBAF3)
147:144	LBA Format 4 Support (LBAF4)
151:148	LBA Format 5 Support (LBAF5)
155:152	LBA Format 6 Support (LBAF6)
159:156	LBA Format 7 Support (LBAF7)
163:160	LBA Format 8 Support (LBAF8)
167:164	LBA Format 9 Support (LBAF9)
171:168	LBA Format 10 Support (LBAF10)
175:172	LBA Format 11 Support (LBAF11)
179:176	LBA Format 12 Support (LBAF12)
183:180	LBA Format 13 Support (LBAF13)
187:184	LBA Format 14 Support (LBAF14)
191:188	LBA Format 15 Support (LBAF15)
383:192	Reserved
4095:384	Vendor Specific (VS)

List of Device Identification for Each Capacity

Capacity (GB)	Byte[7:0]: Namespace Size (NSZE)
128	EE7C2B0h
256	1DCF32B0h
512	3B9E12B0h
1024	773BD2B0h
2048	EE7752B0h

8. SMART Attributes

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1
[203:202]	2	Temperature Sensor 2
[205:204]	2	Temperature Sensor 3
[207:206]	2	Temperature Sensor 4

9. System Power Consumption

■ Supply Voltage

Parameter	Rating
Operating Voltage	3.3V

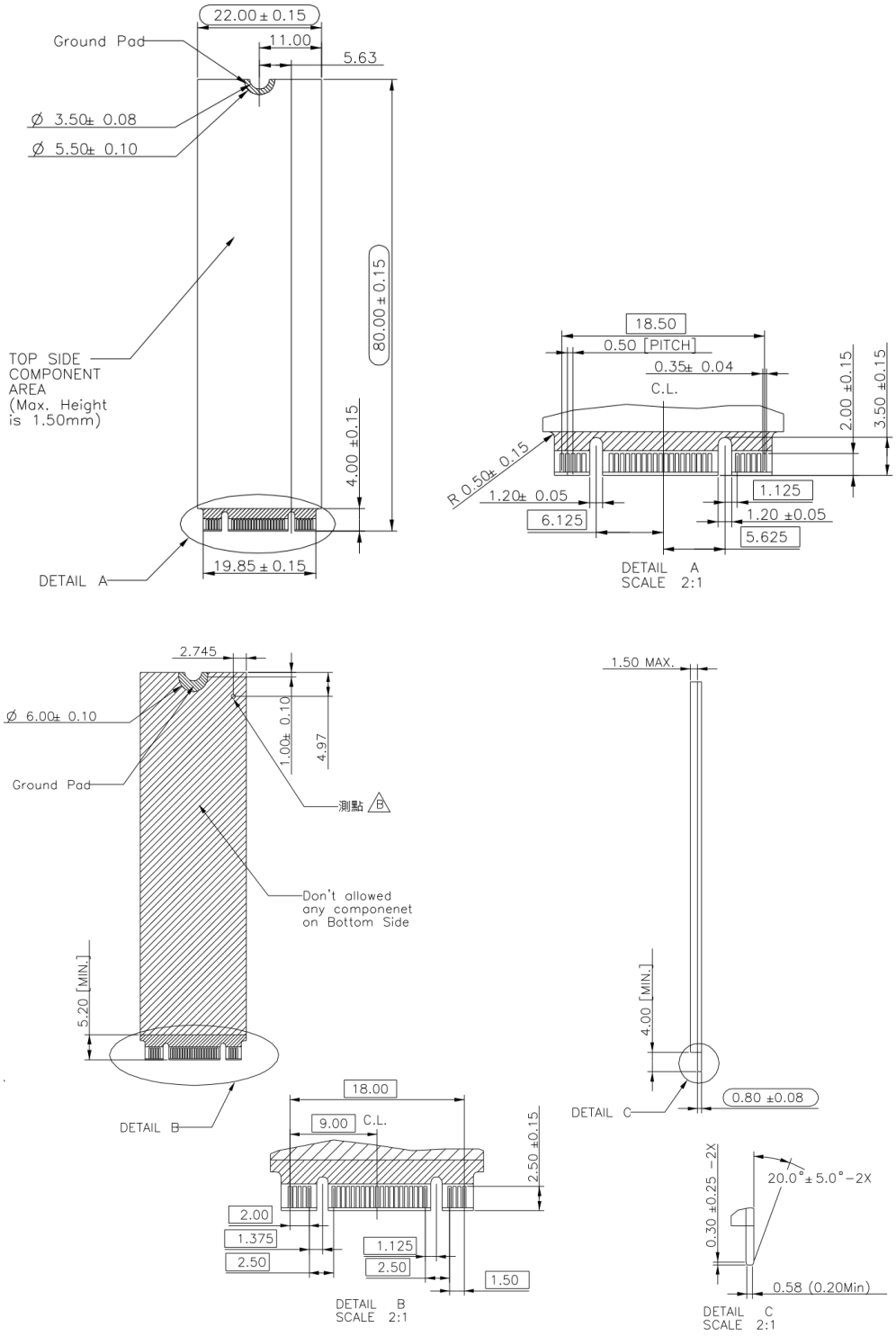
■ Power Consumption

(mW)		Read	Write
3D TLC (BiCS4)	128 GB	2,800	1,900
	256 GB	3,000	2,400
	512 GB	3,300	3,000
	1 TB	3,500	3,200
	2 TB	3,800	3,600

1. Use CrystalDiskMark 6.0.0 with the setting of 1GB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5]
2. Power Consumption may differ according to flash configuration and platform.
3. The measured power voltage is 3.3V.

10. Physical Dimension

M.2 2280 (B+M key) PCIe/NVMe SSD (Unit: mm)



Appendix: Part Number Table

Product	Advantech PN
SQF 720-C PCIe/NVMe M.2 2280 (B+M Key) 128G 3D TLC BiCS4 (0~70°C)	SQF-C8BV2-128GCEDC
SQF 720-C PCIe/NVMe M.2 2280 (B+M Key) 256G 3D TLC BiCS4 (0~70°C)	SQF-C8BV2-256GCEDC
SQF 720-C PCIe/NVMe M.2 2280 (B+M Key) 512G 3D TLC BiCS4 (0~70°C)	SQF-C8BV4-512GCEDC
SQF 720-C PCIe/NVMe M.2 2280 (B+M Key) 1T 3D TLC BiCS4 (0~70°C)	SQF-C8BV4-1TCEDC
SQF 720-C PCIe/NVMe M.2 2280 (B+M Key) 2T 3D TLC BiCS4 (0~70°C)	SQF-C8BV4-2TCEDC