

# **M.2 2280 PCIe SSD 920-C Datasheet**

**(SQF-CM8xx-xxxGCECC)**

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## Revision History

| Rev. | Date     | History                |
|------|----------|------------------------|
| 1.0  | 2021/4/5 | 1. Preliminary release |
| 1.1  | 2021/5/2 | 1. Add test result     |
|      |          |                        |
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**Safety Instructions**

1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
5. Keep this equipment away from humidity.
6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. **DO NOT COVER THE OPENINGS.**
8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
12. Never pour any liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following situations arises, get the equipment checked by service personnel:
  - The power cord or plug is damaged.
  - Liquid has penetrated the equipment.
  - The equipment has been exposed to moisture.
  - The equipment does not work well, or you cannot get it to work according to the user's manual.
  - The equipment has been dropped and damaged.
  - The equipment has obvious signs of breakage.
15. **DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C (-4° F) OR ABOVE 60° C (140° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.**
16. **CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.**

**Consignes de sécurité**

1. Lisez attentivement ces instructions de sécurité.
2. Conservez ce manuel pour référence ultérieure.
3. Débranchez cet appareil de toute prise secteur avant le nettoyage. Utilisez un chiffon humide. Ne pas utiliser de détergents liquides ou en aérosol pour le nettoyage
4. Pour les équipements enfichables, la prise de courant doit être située près de l'équipement et doit être facilement accessible.
5. Gardez cet équipement à l'abri de l'humidité.
6. Placez cet équipement sur une surface fiable lors de l'installation. Le laisser tomber ou le laisser tomber peut causer des dommages.
7. Les ouvertures sur l'enceinte sont destinées à la convection de l'air. Protégez l'équipement de la surchauffe. **NE COUVREZ PAS LES OUVERTURES.**
8. Assurez-vous que la tension de la source d'alimentation est correcte avant de connecter l'équipement à la prise de courant.
9. Positionnez le cordon d'alimentation de sorte que personne ne puisse marcher dessus. Ne placez rien sur le cordon d'alimentation.
10. Toutes les mises en garde et avertissements sur l'équipement doivent être notés..
11. Si l'appareil n'est pas utilisé pendant une longue période, débranchez-le de la source d'alimentation pour éviter tout dommage dû à une surtension transitoire.
12. Ne jamais verser de liquide dans une ouverture. Cela pourrait provoquer un incendie ou un choc électrique.
13. N'ouvrez jamais l'équipement. Pour des raisons de sécurité, l'équipement ne doit être ouvert que par du personnel qualifié.
14. Si l'une des situations suivantes se produit, faites vérifier l'équipement par le personnel de service:!
  - Le cordon d'alimentation ou la fiche est endommagé Liquid has penetrated the equipment.
  - L'équipement a été exposé à l'humidité.
  - L'équipement ne fonctionne pas bien ou vous ne pouvez pas le faire fonctionner conformément au manuel d'utilisation..
  - L'équipement est tombé et endommagé..
  - L'équipement présente des signes évidents de rupture.
15. **NE PAS LAISSER CET APPAREIL DANS UN ENVIRONNEMENT O LA TEMPÉRATURE DE STOCKAGE PEUT ÊTRE INFÉRIEURE À -20 ° C (-4 ° F) OU SUPÉRIEURE À 60 ° C (140 ° F). CELA POURRAIT ENDOMMAGER L'ÉQUIPEMENT. L'ÉQUIPEMENT DOIT ÊTRE DANS UN ENVIRONNEMENT CONTRÔLÉ.**
16. **ATTENTION: DANGER D'EXPLOSION EN CAS DE REMPLACEMENT INCORRECT DE LA PILE. REMPLACEZ UNIQUEMENT AVEC LE MÊME TYPE OU LE TYPE ÉQUIVALENT RECOMMANDÉ PAR LE FABRICANT, DÉJETTEZ LES PILES UTILISÉES SELON LES INSTRUCTIONS DU FABRICANT.**

Specifications subject to change without notice, contact your sales representatives for the most update information.

## 1. Overview

Advantech SQFlash 920-C series M.2 2280 PCIe SSD (Solid State Drive) delivers all the advantages of flash disk technology with PCIe Gen3 x4 interface, including being compliant with standard M.2 2280 (M Key) form factor. The device is designed to operate at a maximum operating frequency of 200MHz with 25MHz external crystal. Its capacity could provide a wide range up to 1.9TB. Moreover, it can reach up to 3,400MB/s read as well as 2,700MB/s write high performance based on Kioxia 96-layer 3D TLC Flash.

## **2. Features**

### **■ PCIe Interface**

- Compliant with NVMe1.3
- Compatible with PCIe I/II/III x4 interface
- Support up to queue depth 64K
- Support power management

### **■ Operating Voltage : 3.3V**

### **■ Support LDPC with RAID ECC**

### **■ AES256 、TCG-OPAL 、TRIM 、AHCI supported**

### **■ Hardware Quick Erase supported (optional)**

### **■ Voltage Stabilizer supported (optional)**

### **■ Temperature Ranges**

- Commercial Temperature
  - 0°C to 70°C for operating
  - -40°C to 85°C for storage

### **■ Mechanical Specification**

- Shock : 1,500G / 0.5ms
- Vibration : 20G / 80~2,000Hz

### **■ Humidity**

- Humidity : 5% ~ 95% under 55°C

### **■ Acquired RoHS 、WHQL 、CE 、FCC Certificate**

### **■ Acoustic : 0 dB**

### **■ Dimension : 80.0 mm x 22.0 mm x 7.3 mm**

### 3. Specification Table

#### ■ Performance

|                   |         | Sequential (MB/sec) |       | Random (IOPS @4K) |       |
|-------------------|---------|---------------------|-------|-------------------|-------|
|                   |         | Read                | Write | Read              | Write |
| 3D TLC<br>(BiCS4) | 240 GB  | 3,200               | 1,300 | 215K              | 320K  |
|                   | 480 GB  | 3,400               | 2,400 | 420K              | 635K  |
|                   | 960 GB  | 3,400               | 3,100 | 700K              | 690K  |
|                   | 1920 GB | 3,400               | 3,000 | 700K              | 680k  |

\* Performance measured by IOMeter with QD32, 8GB data pattern, SLC pool enable & adjustable by request.

## ■ Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a SSD can be written which is a measurement of SSDs' expected lifespan, represents the amount of data written to the device.

$$TBW = [(NAND\ Endurance) \times (SSD\ Capacity)] / WAF$$

- **NAND Endurance:** Program / Erase cycle of a NAND flash.
  - SLC: 100,000 cycles
  - Ultra MLC: 30,000 cycles
  - MLC: 3,000 cycles
  - 3D TLC (BiCS3/ BiCS4): 3,000 cycles
- **SSD Capacity:** SSD physical capacity in total of a SSD.
- **WAF:** Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

$$WAF = (Lifetime\ write\ to\ flash) / (Lifetime\ write\ to\ host)$$

- **Endurance measurement is based on New JEDEC 219 Client Workload and verified with following workload conditions,**
  - PreCond%full = 100%
  - Trim commands enabled
  - Random data pattern.

| 3D TLC (BiCS4) | WAF | TBW  | DWPD* |
|----------------|-----|------|-------|
| 240 GB         | 2.6 | 270  | 1.02  |
| 480 GB         | 2.4 | 580  | 1.10  |
| 960 GB         | 2.4 | 1180 | 1.12  |
| 1920 GB        | 2.3 | 2400 | 1.14  |

\* Endurance of 1 drive writes per day (DWPD) for 3 years

## 4. General Description

### ■ Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, SQFlash 920-C series PCIe SSD applies the LDPC with RAID ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

### ■ Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

SQFlash provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

### ■ Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. SQFlash implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

### ■ Power Loss Protection

#### – Flush Manager

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, SQFlash SSD applies the Flush Manager technology, only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

In addition, it is critical for a controller to shorten the time the in-flight data stays in the controller internal cache. Thus, SQFlash applies an algorithm to reduce the amount of data resides in the cache to provide a better performance. With Flush Manager, incoming data would only have a “pit stop” in the cache and then move to NAND flash directly. Also, the onboard DDR will be treated as an “organizer” to consolidate incoming data into groups before written into the flash to improve write amplification.

#### – Voltage Stabilizer

While the built-in voltage detector detects an unstable power input ( $< 3.135\text{ V}$  or  $> 3.465\text{ V}$ ), the controller will issue a power failure interrupt and force a Flush CMD first. At the same time, the whole internal power supply will be switched to Voltage Stabilizer immediately to ensure stable power is supplied throughout the whole drive. This ensures the Flash IC and DDR IC will not operate with unstable power which could lead to data errors or bad data integrity.

### ■ TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

**■ SMART**

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

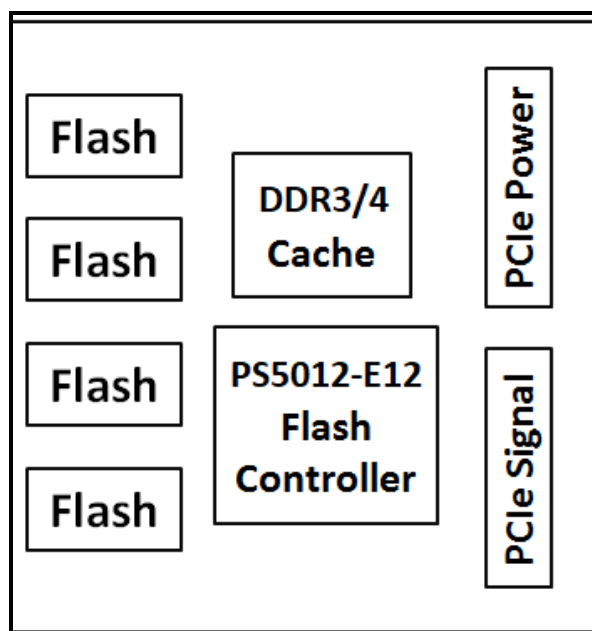
**■ Over-Provision**

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

**■ Thermal Throttling**

Thermal Throttling function is for protecting the drive and reducing the possibility of read / write error due to overheat. The temperature is monitored by the thermal sensor. As the operating temperature continues to increase to threshold temperature, the Thermal Throttling mechanism is activated. At this time, the performance of the drive will be significantly decreased to avoid continuous heating. When the operating temperature falls below threshold temperature, the drive can resume to normal operation.

## ■ Block Diagram



## ■ LBA value

| Density (GB) | LBA           |
|--------------|---------------|
| 240          | 468,862,128   |
| 480          | 937,703,088   |
| 960          | 1,875,385,008 |
| 1920         | 3,750,748,848 |

## 5. Security Features

### ■ **Advanced Encryption Standard (AES)**

An AES 256-bit encryption key is generated in the drive's security controller before the data got stored on the NAND flash. When the controller or firmware fails, the data that is securely stored in the encryption key becomes inaccessible through the NAND flash.

### ■ **TCG-OPAL 2.0 Compliance**

TCG-OPAL compliance SED (Self-encryption Drive) supports a built-in shadow MBR to process user authentication to SSD before booting to normal MRR area and OS. SQFlash 920-C series supports such feature with 100% TCG-OPAL compliance. Further, with SQFlash Flash Lock function, the user authentication process in shadow MBR can be done automatically by bonding with motherboard unique ID such as UUID in BIOS / MAC address / TPM unique code. So with Flash Lock enabled, only designated motherboard can have access to the SSD.

### ■ **Flash Vault**

Flash Vault is to lock Read and Write command by SSD firmware setting and make the SSD need password to verify and only operate with the corresponding platform. User can use Flash Vault to prevent data being stolen by reading the SQFlash SSD with other computers and unauthorized person.

### ■ **Security ID**

Security ID is to encrypt user's specific application software encryption. To enable this function, the application software is required to build Security ID function code and user needs to enable the firmware function by entering Access Code of SQFlash Utility, and then the Security ID can be set. When Security ID sets, the application software is protected by Security ID and SQFlash Utility

## 6. Pin Assignment and Description

| Pin No. | PCIe Pin               | Description                                                                               |
|---------|------------------------|-------------------------------------------------------------------------------------------|
| 1       | GND                    | Ground                                                                                    |
| 2       | 3.3V                   | 3.3V source                                                                               |
| 3       | GND                    | Ground                                                                                    |
| 4       | 3.3V                   | 3.3V source                                                                               |
| 5       | PETn3                  | PCIe TX Differential signal defined by the PCIe 3.0 specification                         |
| 6       | N/C                    | No connect                                                                                |
| 7       | PETp3                  | PCIe TX Differential signal defined by the PCIe 3.0 specification                         |
| 8       | N/C                    | No connect                                                                                |
| 9       | GND                    | Ground                                                                                    |
| 10      | LED1#(O)               | Status indicators via LED devices                                                         |
| 11      | PERn3                  | PCIe RX Differential signal defined by the PCIe 3.0 specification                         |
| 12      | 3.3V                   | 3.3V source                                                                               |
| 13      | PERp3                  | PCIe RX Differential signals defined by the PCIe 3.0 specification.                       |
| 14      | 3.3V                   | 3.3V source                                                                               |
| 15      | GND                    | Ground                                                                                    |
| 16      | 3.3V                   | 3.3V source                                                                               |
| 17      | PETn2                  | PCIe TX Differential signal defined by the PCIe 3.0 specification                         |
| 18      | 3.3V                   | 3.3V source                                                                               |
| 19      | PETp2                  | PCIe TX Differential signal defined by the PCIe 3.0 specification                         |
| 20      | N/C                    | No connect                                                                                |
| 21      | GND                    | Ground                                                                                    |
| 22      | N/C                    | No connect                                                                                |
| 23      | PERn2                  | PCIe RX Differential signal defined by the PCIe 3.0 specification                         |
| 24      | N/C                    | No connect                                                                                |
| 25      | PERp2                  | PCIe RX Differential signal defined by the PCIe 3.0 specification                         |
| 26      | N/C                    | No connect                                                                                |
| 27      | GND                    | Ground                                                                                    |
| 28      | N/C                    | No connect                                                                                |
| 29      | PETn1                  | PCIe TX Differential signal defined by the PCIe 3.0 specification                         |
| 30      | N/C                    | No connect                                                                                |
| 31      | PETp1                  | PCIe TX Differential signal defined by the PCIe 3.0 specification                         |
| 32      | N/C                    | No connect                                                                                |
| 33      | GND                    | Ground                                                                                    |
| 34      | N/C                    | No connect                                                                                |
| 35      | PERn1                  | PCIe RX Differential signal defined by the PCIe 3.0 specification                         |
| 36      | N/C                    | No connect                                                                                |
| 37      | PERp1                  | PCIe RX Differential signal defined by the PCIe 3.0 specification                         |
| 38      | N/C                    | No connect                                                                                |
| 39      | GND                    | Ground                                                                                    |
| 40      | SMB_CLK (I/O)(0/1.8V)  | SMBus Clock; Open Drain with pull-up on platform (Reserve)                                |
| 41      | PETn0                  | PCIe TX Differential signal defined by the PCIe 3.0 specification                         |
| 42      | SMB_DATA (I/O)(0/1.8V) | SMBus Data; Open Drain with pull-up on platform (Reserve)                                 |
| 43      | PETp0                  | PCIe TX Differential signal defined by the PCIe 3.0 specification                         |
| 44      | N/C                    | No connect                                                                                |
| 45      | GND                    | Ground                                                                                    |
| 46      | N/C                    | No connect                                                                                |
| 47      | PERn0                  | PCIe RX Differential signal defined by the PCIe 3.0 specification                         |
| 48      | N/C                    | No connect                                                                                |
| 49      | PERp0                  | PCIe RX Differential signal defined by the PCIe 3.0 specification                         |
| 50      | PERST#(I)(0/3.3V)      | PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification. |
| 51      | GND                    | Ground                                                                                    |

Specifications subject to change without notice, contact your sales representatives for the most update information.

|    |                        |                                                                                                                                            |
|----|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 52 | CLKREQ#(I/O)(0/3.3V)   | Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Substates.             |
| 53 | REFCLKn                | PCIe Reference Clock signals (100 MHz) defined by the PCIe 3.0 specification.                                                              |
| 54 | PEWAKE#(I/O)(0/3.3V)   | PCIe PME Wake.<br>Open Drain with pull up on platform; Active Low.                                                                         |
| 55 | REFCLKp                | PCIe Reference Clock signals (100 MHz) defined by the PCIe 3.0 specification.                                                              |
| 56 | Reserved for MFG DATA  | Manufacturing Data line. Used for SSD manufacturing only.<br>Not used in normal operation.<br>Pins should be left N/C in platform Socket.  |
| 57 | GND                    | Ground                                                                                                                                     |
| 58 | Reserved for MFG CLOCK | Manufacturing Clock line. Used for SSD manufacturing only.<br>Not used in normal operation.<br>Pins should be left N/C in platform Socket. |
| 59 | Module Key             | Module Key                                                                                                                                 |
| 60 | Module Key             |                                                                                                                                            |
| 61 | Module Key             |                                                                                                                                            |
| 62 | Module Key             |                                                                                                                                            |
| 63 | Module Key             |                                                                                                                                            |
| 64 | Module Key             |                                                                                                                                            |
| 65 | Module Key             |                                                                                                                                            |
| 66 | Module Key             |                                                                                                                                            |
| 67 | N/C                    | No connect                                                                                                                                 |
| 68 | N/C                    | No connect                                                                                                                                 |
| 69 | PEDET (NC-PCIe)        | Host I/F Indication; No Connect for PCIe.                                                                                                  |
| 70 | 3.3V                   | 3.3V source                                                                                                                                |
| 71 | GND                    | Ground                                                                                                                                     |
| 72 | 3.3V                   | 3.3V source                                                                                                                                |
| 73 | GND                    | Ground                                                                                                                                     |
| 74 | 3.3V                   | 3.3V source                                                                                                                                |
| 75 | GND                    | Ground                                                                                                                                     |

## 7. NVMe Command List

### ■ Admin commands

| Opcode                          | Command Description         |
|---------------------------------|-----------------------------|
| 00h                             | Delete I/O Submission Queue |
| 01h                             | Create I/O Submission Queue |
| 02h                             | Get Log Page                |
| 04h                             | Delete I/O Completion Queue |
| 05h                             | Create I/O Completion Queue |
| 06h                             | Identify                    |
| 08h                             | Abort                       |
| 09h                             | Set Features                |
| 0Ah                             | Get Features                |
| 0Ch                             | Asynchronous Event Request  |
| 10h                             | Firmware Activate           |
| 11h                             | Firmware Image Download     |
| <b>I/O Command Set Specific</b> |                             |
| 80h                             | Format NVM                  |
| 81h                             | Security Send               |
| 82h                             | Security Receive            |
| 83h-BFh                         | I/O Command Set specific    |
| <b>Vendor Specific</b>          |                             |
| C0h-FFh                         | Vendor specific             |

### ■ NVM commands

| Opcode                 | Command Description  |
|------------------------|----------------------|
| 00h                    | Flush                |
| 01h                    | Write                |
| 02h                    | Read                 |
| 04h                    | Write Uncorrectable  |
| 05h                    | Compare              |
| 08h                    | Write Zeroes         |
| 09h                    | Dataset Management   |
| 0Dh                    | Reservation Register |
| 0Eh                    | Reservation Report   |
| 11h                    | Reservation Acquire  |
| 15h                    | Reservation Release  |
| <b>Vendor Specific</b> |                      |
| 80h – FFh              | Vendor specific      |

## 8. Identify Device Data

The Identify Device Data enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero

### ■ Identify Controller Data Structure

| Bytes                                                                      | Description                                                         |
|----------------------------------------------------------------------------|---------------------------------------------------------------------|
| <b>Controller Capabilities and Features</b>                                |                                                                     |
| 01:00                                                                      | PCI Vendor ID (VID)                                                 |
| 03:02                                                                      | PCI Subsystem Vendor ID (SSVID)                                     |
| 23:04                                                                      | Serial Number (SN)                                                  |
| 63:24                                                                      | Model Number (MN)                                                   |
| 71:64                                                                      | Firmware Revision (FR)                                              |
| 72                                                                         | Recommended Arbitration Burst (RAB)                                 |
| 75:73                                                                      | IEEE OUI Identifier (IEEE)                                          |
| 76                                                                         | Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC) |
| 77                                                                         | Maximum Data Transfer Size (MDTS)                                   |
| 255:80                                                                     | Reserved                                                            |
| <b>Admin Command Set Attributes &amp; Optional Controller Capabilities</b> |                                                                     |
| 257:256                                                                    | Optional Admin Command Support (OACS)                               |
| 258                                                                        | Abort Command Limit (ACL)                                           |
| 259                                                                        | Asynchronous Event Request Limit (AERL)                             |
| 260                                                                        | Firmware Updates (FRMW)                                             |
| 261                                                                        | Log Page Attributes (LPA)                                           |
| 262                                                                        | Error Log Page Entries (ELPE)                                       |
| 263                                                                        | Number of Power States Support (NPSS)                               |
| 264                                                                        | Admin Vendor Specific Command Configuration (AVSCC)                 |
| 265                                                                        | Autonomous Power State Transition Attributes (APSTA)                |
| 511:266                                                                    | Reserved                                                            |
| <b>NVM Command Set Attributes</b>                                          |                                                                     |
| 512                                                                        | Submission Queue Entry Size (SQES)                                  |
| 513                                                                        | Completion Queue Entry Size (CQES)                                  |
| 515:514                                                                    | Reserved                                                            |
| 519:516                                                                    | Number of Namespaces (NN)                                           |
| 521:520                                                                    | Optional NVM Command Support (ONCS)                                 |
| 523:522                                                                    | Fused Operation Support (FUSES)                                     |
| 524                                                                        | Format NVM Attributes (FNA)                                         |
| 525                                                                        | Volatile Write Cache (VWC)                                          |
| 527:526                                                                    | Atomic Write Unit Normal (AWUN)                                     |
| 529:528                                                                    | Atomic Write Unit Power Fail (AWUPF)                                |
| 530                                                                        | NVM Vendor Specific Command Configuration (NVSCC)                   |
| 531                                                                        | Reserved                                                            |
| 533:532                                                                    | Atomic Compare & Write Unit (ACWU)                                  |
| 535:534                                                                    | Reserved                                                            |
| 539:536                                                                    | SGL Support (SGLS)                                                  |
| 703:540                                                                    | Reserved                                                            |

## ■ Identify Namespace Data Structure & NVM Command Set Specific

| Bytes    | Description                                                        |
|----------|--------------------------------------------------------------------|
| 7:0      | Namespace Size (NSZE)                                              |
| 15:8     | Namespace Capacity (NCAP)                                          |
| 23:16    | Namespace Utilization (NUSE)                                       |
| 24       | Namespace Features (NSFEAT)                                        |
| 25       | Number of LBA Formats (NLBAF)                                      |
| 26       | Formatted LBA Size (FLBAS)                                         |
| 27       | Metadata Capabilities (MC)                                         |
| 28       | End-to-end Data Protection Capabilities (DPC)                      |
| 29       | End-to-end Data Protection Type Settings (DPS)                     |
| 30       | Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC) |
| 31       | Reservation Capabilities (RESCAP)                                  |
| 119:32   | Reserved                                                           |
| 127:120  | IEEE Extended Unique Identifier (EUI64)                            |
| 131:128  | LBA Format 0 Support (LBAF0)                                       |
| 135:132  | LBA Format 1 Support (LBAF1)                                       |
| 139:136  | LBA Format 2 Support (LBAF2)                                       |
| 143:140  | LBA Format 3 Support (LBAF3)                                       |
| 147:144  | LBA Format 4 Support (LBAF4)                                       |
| 151:148  | LBA Format 5 Support (LBAF5)                                       |
| 155:152  | LBA Format 6 Support (LBAF6)                                       |
| 159:156  | LBA Format 7 Support (LBAF7)                                       |
| 163:160  | LBA Format 8 Support (LBAF8)                                       |
| 167:164  | LBA Format 9 Support (LBAF9)                                       |
| 171:168  | LBA Format 10 Support (LBAF10)                                     |
| 175:172  | LBA Format 11 Support (LBAF11)                                     |
| 179:176  | LBA Format 12 Support (LBAF12)                                     |
| 183:180  | LBA Format 13 Support (LBAF13)                                     |
| 187:184  | LBA Format 14 Support (LBAF14)                                     |
| 191:188  | LBA Format 15 Support (LBAF15)                                     |
| 383:192  | Reserved                                                           |
| 4095:384 | Vendor Specific (VS)                                               |

## ■ List of Device Identification for Each Capacity

| Capacity (GB) | Byte[7:0]: Namespace Size (NSZE) |
|---------------|----------------------------------|
| 240           | 1BF244B0h                        |
| 480           | 37E436B0h                        |
| 960           | 6FC81AB0h                        |
| 1920          | DF8FE2B0h                        |

## 9. System Power Consumption

### ■ Supply Voltage

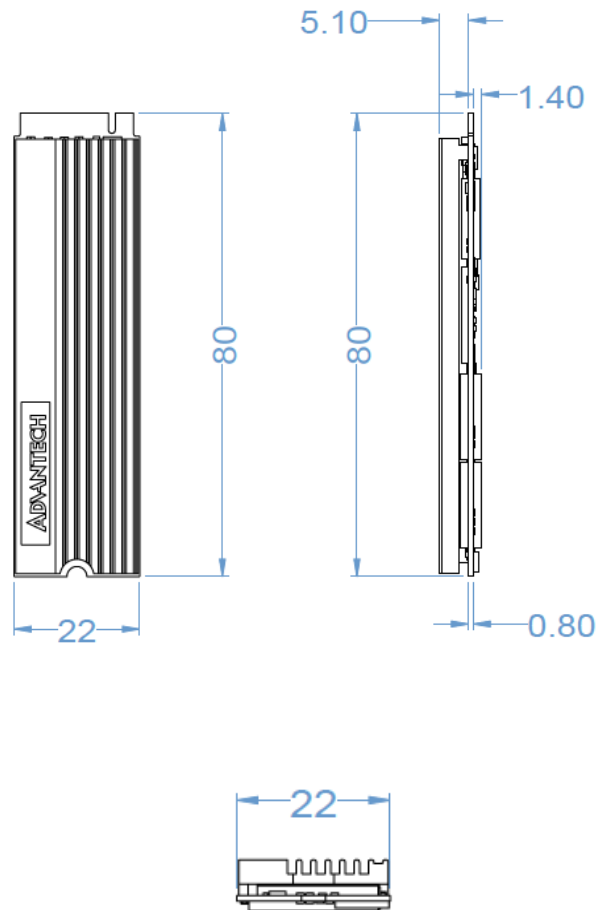
| Parameter         | Rating |
|-------------------|--------|
| Operating Voltage | 3.3V   |

### ■ Power Consumption

| (W)               |         | Read | Write | Idle |
|-------------------|---------|------|-------|------|
| 3D TLC<br>(BiCS4) | 240 GB  | 5.0  | 3.1   | 2.0  |
|                   | 480 GB  | 5.1  | 4.9   | 2.0  |
|                   | 960 GB  | 5.3  | 5.3   | 2.0  |
|                   | 1920 GB | 5.3  | 5.0   | 2.0  |

### 10. Physical Dimension

M.2 2280 PCIe SSD (Unit: mm)



## Appendix: Part Number Table

| Product                                                          | Advantech PN       |
|------------------------------------------------------------------|--------------------|
| SQF 920-C NVMe M.2 2280 SSD (OPAL) 240G 3D TLC (BiCS4) (0~70°C)  | SQF-CM8V4-240GCECC |
| SQF 920-C NVMe M.2 2280 SSD (OPAL) 480G 3D TLC (BiCS4) (0~70°C)  | SQF-CM8V4-480GCECC |
| SQF 920-C NVMe M.2 2280 SSD (OPAL) 960G 3D TLC (BiCS4) (0~70°C)  | SQF-CM8V4-960GCECC |
| SQF 920-C NVMe M.2 2280 SSD (OPAL) 1920G 3D TLC (BiCS4) (0~70°C) | SQF-CM8V4-1K9GCECC |