M.2 2230 PCIe/NVMe SSD 730-D Datasheet

(SQF-C3Mxx-xxxGDEFx) (M Key)

CONTENTS

Revision History

Rev.	Date	History
0.1	2023/4/25	1. Preliminary
0.2	2024/07/09	1. Modify SMART information

1. Overview

Advantech SQFlash 730-D series M.2 2230 (M Key) PCIe/NVMe SSD (Solid State Drive) delivers all the advantages of flash disk technology with PCIe Gen. 4x4 interface, including being fully compliant with the standard Next Generation Form Factor (NGFF) M.2 2230 form factor, providing low power consumption compared to traditional hard drive and hot-swapping when removing/replacing/upgrading flash disks. The device is designed based on the M.2 2230 standard. SQFlash 730-D M.2 2230 SSD offers up to 512GB and its performance can reach up to 4,900MB/s read as well as 3,300MB/s write high performance based on Kioxia 112L 3D TLC NAND flash.

2. Features

- **PCIe Interface**
  - Compliant with NVMe 1.4
  - PCI Express Base 4.0
  - PCIe Gen. 4x4 lane & backward compatible to PCIe Gen3, Gen 2 and Gen 1
  - Support up to QD 128 with queue depth of up to 64K
- **Operating Voltage：3.3V**
- **Support LDPC of ECC algorithm**
- **Support SMART and TRIM commands**
- **Temperature Ranges[1]**
  - Commercial Temperature
    - 0℃ to 70℃ for operating
    - -40℃ to 85℃ for storage
  - Industrial Temperature
    - -40℃ to 85℃ for operating
    - -40℃ to 85℃ for storage

*Note : 1. Based on SMART Attribute (Byte index [2 :1] of PCIe-SIG standard, which measured by thermal sensor

- **Mechanical Specification**
  - Shock：1,500G / 0.5ms
  - Vibration：20G / 80~2,000Hz
- **Humidty**
  - Humidity：up to 95% on 40℃
- **Acquired RoHS、WHQL、CE、FCC Certificate**
- **Acoustic：0 dB**
- **Dimension：30.0 mm x 22.0 mm x 2.15 mm**

3. Specification Table

■ Performance

SQF-C3M (DEFC)

		Sequential Performance (MB/sec)		Random Performance (IOPS @4K)	
		Read	**Write**	**Read**	**Write**
3D TLC (BiCS5)	256 GB	3,800	1,700	200K	400K
	512 GB	4,900	3,300	320K	600K

SQF-C3M (DEFE)

		Sequential Performance (MB/sec)		Random Performance (IOPS @4K)	
		Read	**Write**	**Read**	**Write**
3D TLC (BiCS5)	256 GB	3,000	1,100	110K	245K
	512 GB	3,700	2,000	220K	450K

NOTES:

1. The performance was estimated based on Kioxia 3D TLC BICS5 flash.
2. Performance may differ according to flash configuration and platform.
3. Use CrystalDiskMark 7.0.0 with QD8T1, 1GB range for sequential read/write test.
4. Use IOmeter v1.1.0 with QD32T16, 1GB range for 4KB random read/write test.
5. Performance specification is under that Thermal Throttling has not worked yet.
6. CPU: AMD Ryzen 7 5800X 8-Core Processor
7. Operating System: Windows 10 Professional (x64)

■ Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a SSD can be written which is a measurement of SSDs' expected lifespan, represents the amount of data written to the device.

TBW = [(NAND Endurance) x (SSD Capacity)] / WAF

- **NAND Endurance**: Program / Erase cycle of a NAND flash.
    - 3D TLC (BiCS3/ BiCS4/ BiCS5): 3,000 cycles
    - 3D sTLC (BiCS4): 30,000 cycles
    - 3D sTLC (BiCS5): 50,000 cycles
- **SSD Capacit**y: SSD physical capacity in total of a SSD.
- **WAF**: Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

WAF = (Lifetime write to flash) / (Lifetime write to host)

Endurance measurement is based on JEDEC 219A client workload and verified with following workload conditions,

- PreCond%full = 100%
- Trim commands enabled
- Random data pattern.

Capacity	TBW
	3D TLC (BiCS5)
256 GB	248
512 GB	661

4. General Description

■ Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, SQF-C3M 730-D applies the LDPC algorithm, which can detect and correct data errors even with the latest 3D TLC technology to ensure data being read correctly, and protects data from corruption.

■ Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, when flash media is not used evenly, some blocks get updated more frequently than others and the lifetime of device would be reduced significantly. Thus, wear leveling is applied to extend the lifespan of NAND flash by evenly distributing write and erase cycles across the media.

SQFlash 730-D series provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static wear leveling algorithms, the life expectancy of the NAND flash is greatly improved.

■ Bad Block Management

Bad blocks are blocks that do not function properly or contain more invalid bits causing stored data unstable, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Early Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. SQFlash 730-D series implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages bad blocks that appear with use. This practice prevents data being stored into bad blocks and further improves the data reliability.

■ Power Loss Protection: Flush Manager

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, SQFlash SSD applies the Flush Manager technology, only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

In addition, it is critical for a controller to shorten the time the in-flight data stays in the controller internal cache. Thus, SQFlash applies an algorithm to reduce the amount of data resides in the cache to provide a better performance. With Flush Manager, incoming data would only have a “pit stop” in the cache and then move to NAND flash directly. Also, the onboard DDR will be treated as an “organizer” to consolidate incoming data into groups before written into the flash to improve write amplification.

■ TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD so that blocks of data that are no longer in use can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks at all time.

■ SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a solid state drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users impending failures while there is still time to perform proactive actions, such as save data to another device.

Over-Provision

Over Provisioning refers to the preserving additional area beyond user capacity in a SSD, which is not visible to users and cannot be used by them. However, it allows a SSD controller to utilize additional space for better performance and WAF. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

Thermal Throttling

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. Thermal Throttling function is for protecting the drive and reducing the possibity of read / write error due to overheat. The temperature is monitored by the thermal sensor. As the operating temperature continues to increase to theshold temperature, the Thermal Throttling mechanism is activated. At this time, the performance of the drive will be significantly decreased to avoid continuous heating. When the operating temperature falls below theshold temperutue, the drive can resume to normal operation.

Advanced Device Security Features

Advanced Encryption Standard (AES)

An AES 256-bit encryption key is generated in the drive's security controller before the data gets stored on the NAND flash. When the controller or firmware fails, the data that is securely stored in the encryption key becomes inaccessible through the NAND flash.

OPAL 2.0 support

SQFlash 730-D series supports standard OPAL 2.0 function for advance Self-Encryption Drive (SED) feature sets. Advantech provides also user friendly interface for setting disk / system bonding to prevent SSD be used in non-authorized platforms, which is called Flash Lock function.

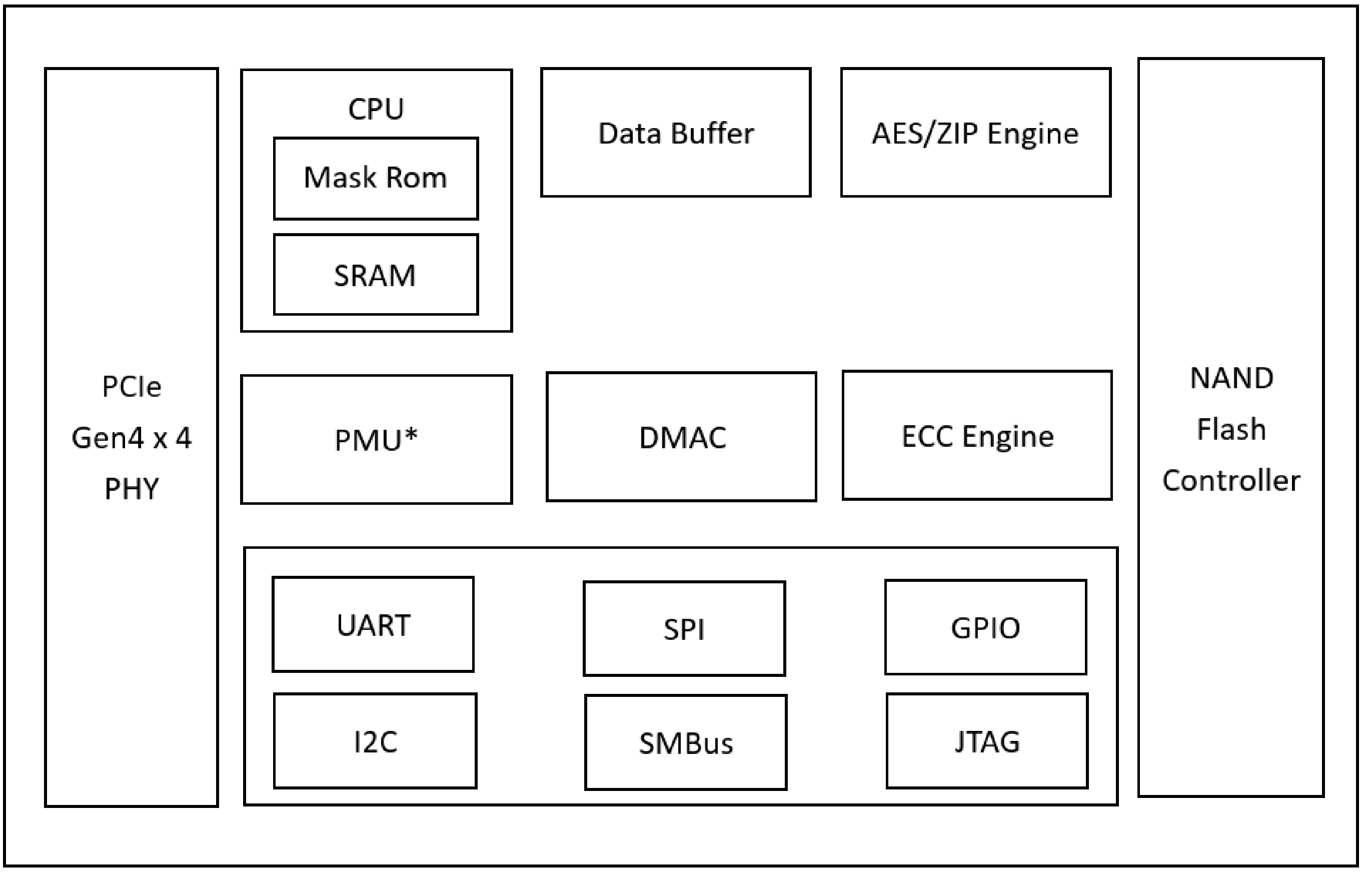
Secure Erase Function

SQFlash 730-D series supports standard NVMe command for secure erase function; when the SSD controller receive the secure erase command, the erase process will reset all blocks and erase all of the user data in the SSD.

Sanitize Fucntion

SQFlash 730-D series default implement NVMe Sanitize Device Feature set, which supports the command set of Block Erase, Overwritten and Crypto Scramble. With the internal AES encryption support, the Crypto Scrambel process will start with resetting AES key. By doing so, existing data will be scrambled within 10ms and cannot be recovered anymore. Moreover, erase flag is set when erase function is triggered, which will ensure the whole erase process can be 100% completed. Even there’s power interrupt, after power resume, erase operation will be resume right away as well.

■ Block Diagram



■ LBA value

Density	LBA
256 GB	500,118,192
512 GB	1,000,215,216

5. Pin Assignment and Description

■ Interface Pin Assignments

Below table defines the signal assignment of the internal NGFF connector for SSD usage, described in the PCI Express M.2 Specification version 1.0 of the PCI-SIG.

Pin No.	PCIe Pin	Description
1	GND	Ground
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	NC	No connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	PLN# (0/3.3V)	Power Loss Notification
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec
20	NC	No connect
21	GND	Ground
22	NC	No connect
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	NC	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	NC	No connect. Reserve for GPIO WP customized
27	GND	Ground
28	NC	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	PLA_S3# (0/3.3V)	No connect
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	NC	No connect
33	GND	Ground
34	NC	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	NC	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	NC	No connect
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA(I/O)(0/1.8V)	SMBus Data; Open Drain with pull-up on platform
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#(O)(0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active low.
45	GND	Ground
46	NC	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec

48	NC	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	NC	No connect. Reserve for GPIO Erase customized
68	SUSCLK(32KHz) (I)(0/3.3V)	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module.
69	NC	No connect
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	Ground

6. NVMe Command List

■ Admin commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
0Dh	Namespace Management
10h	Firmware Activate
11h	Firmware Image Download
NVM Command Set Specific	
80h	Format NVM
81h	Security Send
82h	Security Receive

■ NVM commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
08h	Write Zeroes
09h	Dataset Management
0Ch	Verify

7. Identify Device Data

The Identity Device Data enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero

■ Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	SN
63:24	M	Model Number (MN)	Model Number
71:64	M	Firmware Revision (FR)	FW Name
72	M	Recommended Arbitration Burst (RAB)	0x4
75:73	M	IEEE OUI Identifier (IEEE)	Assigned by IEEE/RAC
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x6
79:78	M	Controller ID (CNTLID)	0x0000
83:80	M	Version (VER)	0x10400
87:84	M	RTD3 Resume Latency (RTD3R)	0x186A0
91:88	M	RTD3 Entry Latency (RTD3E)	0x4C4B40
95:92	M	Optional Asynchronous Events Supported (OAES)	0x00000000
99:96	M	Controller Attributes (CTRATT)	0x2
111:100	-	Reserved	0x1
127:112	O	FRU Globally Unique Identifier (FGUID)	0x00
239:128	-	Reserved	0x00
255:240	-	Refer to the NVMe Management Interface Specification for definition	0
257:256	M	Optional Admin Command Support (OACS)	0x17
258	M	Abort Command Limit (ACL)	0x3
259	M	Asynchronous Event Request Limit (AERL)	0x03
260	M	Firmware Updates (FRMW)	0x12
261	M	Log Page Attributes (LPA)	0x1E
262	M	Error Log Page Entries (ELPE)	0x3E
263	M	Number of Power States Support (NPSS)	0x4
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x1
265	O	Autonomous Power State Transition Attributes	0x1

		(APSTA)	
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x15D (Normal-temp) 0x163 (Wide-temp)
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x15F (Normal-temp) 0x166 (Wide-temp)
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x64
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x4000(HMB off)Depend on Disk Size(HMB on)
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x4000(HMB off)Depend on Disk Size(HMB on)
295:280	O	Total NVM Capacity (TNVMCAP)	By capacity
311:296	O	Unallocated NVM Capacity (UNVMCAP)	0x00
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00
317:316	O	Extended Device Self-test Time (EDSTT)	0x1E
318	O	Device Self-test Options (DSTO)	0x00
319	M	Firmware Update Granularity (FWUG)	0x40
321:320	M	Keep Alive Support (KAS)	0x00
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	0x1
325:324	O	Minimum Thermal Management Temperature (MNTMT)	0x111
327:326	O	Maximum Thermal Management Temperature (MXTMT)	0x15F (Normal-temp) 0x166 (Wide-temp)
331:328	O	Sanitize Capabilities (SANICAP)	0xA0000002
335:332	O	Host Memory Buffer Minimum Descriptor Entry Size (HMMINDS)	0x400
337:336	O	Host Memory Buffer Minimum Descriptor Entries (HMMINDS)	0x10
339:338	O	NVM Set Identifier Maximum (NSETIDMAX)	0x0
341:340	O	Endurance Group Identifier Maximum (ENDGIDMAX)	0x0
342	O	ANA Transition Time (ANATT)	0x0
343	O	Asymmetric Namespace Access Capabilities (ANACAP)	0x0
347:344	O	ANA Group Identifier Maximum (ANAGRPMAX)	0x0

351:348	O	Number of ANA Group Identifiers (NANAGRPID)	0x0
355:352	O	Persistent Event Log Size (PELS)	0x60
511:356	-	Reserved	0x00
NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	M	Maximum Outstanding Commands (MAXCMD)	0x100
519:516	M	Number of Namespaces (NN)	0x1
521:520	M	Optional NVM Command Support (ONCS)	0xDF
523:522	M	Fused Operation Support (FUSES)	0x0
524	M	Format NVM Attributes (FNA)	0x0
525	M	Volatile Write Cache (VWC)	0x7
527:526	M	Atomic Write Unit Normal (AWUN)	0xFF
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x0
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x1
531	M	Reserved	0x0
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0
535:534	M	Reserved	0x0
539:536	O	SGL Support (SGLS)	0x0
543:540	O	Maximum Number of Allowed Namespaces (MNAN)	0x0
767:544	-	Reserved	0x00
IO Command Set Attributes			
1023:768	M	NVM Subssystem NVMe Qualified Name (SUBNQN)	0x00
1791:1024	-	Reserved	0x00
2047:1792	-	Refer to the NVMe over Fabrics specification	0x00
2079:2048	M	Power State 0 Descriptor	Disable LPM 0x0081031600401C5200000000000002580000025800000316 Enable LPM 0x0081031600401C5200000000000002580000025800000316
2111:2080	O	Power State 1 Descriptor	Disable LPM 0x0081031600401C5201010101000002580000025800000316 Enable LPM 0x0081031600401C5201010101000002580000025800000316
2143:2112	O	Power State 2 Descriptor	Disable LPM 0 Enable LPM

			0x0081031600401C520202020200000258000000258000000316
2175:2144	O	Power State 3 Descriptor	Disable LPM 0 Enable LPM 0x0081031600401C5203030303000003E8000003E8030003E8
2207:2176	O	Power State 4 Descriptor	Disable LPM 0 Enable LPM 0x0081031600401C52240404040000186A00000138803000032
…	-	(N/A)	0
3071:3040	O	Power State 31 Descriptor	0
Vendor Specific			
4095:3072	O	Vendor Specific (VS)	Vendor Reserved

■ Identify Namespace Data Structure & NVMe Command Set Specific

Bytes	Description
7:0	Namespace Size (NSZE)
15:8	Namespace Capacity (NCAP)
23:16	Namespace Utilization (NUSE)
24	Namespace Features (NSFEAT)
25	Number of LBA Formats (NLBAF)
26	Formatted LBA Size (FLBAS)
27	Metadata Capabilities (MC)
28	End-to-end Data Protection Capabilities (DPC)
29	End-to-end Data Protection Type Settings (DPS)
30	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)
31	Reservation Capabilities (RESCAP)
32	Format Progress Indicator (FPI)
33	Deallocate Logical Block Features (DLFEAT)
35:34	Namespace Atomic Write Unit Normal (NAWUN)
37:36	Namespace Atomic Write Unit Power Fail (NAWUPF)
39:38	Namespace Atomic Compare & Write Unit (NAWWU)
41:40	Namespace Atomic Boundary Size Normal (NABSN)
43:42	Namespace Atomic Boundary Offset (NABO)
45:44	Namespace Atomic Boundary Size Power Fail (NABSPF)
47:46	Namespace Atomic Optimal IO Boundary (NOIOB)
63:48	NVM Capacity (NVMCAP)
103:64	Reserved
119:104	Namespace Globally Unique Identifier (NGUID)
127:120	IEEE Extended Unique Identifier (EUI64)
131:128	LBA Format 0 Support (LBAF0)
135:132	LBA Format 1 Support (LBAF1)
139:136	LBA Format 2 Support (LBAF2)
143:140	LBA Format 3 Support (LBAF3)
147:144	LBA Format 4 Support (LBAF4)
151:148	LBA Format 5 Support (LBAF5)
155:152	LBA Format 6 Support (LBAF6)
159:156	LBA Format 7 Support (LBAF7)
163:160	LBA Format 8 Support (LBAF8)
167:164	LBA Format 9 Support (LBAF9)
171:168	LBA Format 10 Support (LBAF10)
175:172	LBA Format 11 Support (LBAF11)
179:176	LBA Format 12 Support (LBAF12)
183:180	LBA Format 13 Support (LBAF13)
187:184	LBA Format 14 Support (LBAF14)
191:188	LBA Format 15 Support (LBAF15)
383:192	Reserved
4095:384	Vendor Specific (VS)

■ List of Device Identification for Each Capacity

Capacity (GB)	Byte[7:0]: Namespace Size (NSZE)
256	1DCF32B0h
512	3B9E12B0h

8. SMART Attributes

ID	ATTRIBUTE_NAME	Log Identifier	# of Bytes	Byte index	Unit
01h	Critical Warning	02h	1	[0]	-
02h	Composite Temperature	02h	2	[2:1]	°K
03h	Available Spare	02h	1	[3]	%
04h	Available Spare Threshold	02h	1	[4]	%
05h	Percentage Used	02h	1	[5]	%
06h-10h	Reserved	02h		[31:6]	
11h	Data Units Read	02h	16	[47:32]	1000 Sectors
12h	Data Units Written (Host Write)	02h	16	[63:48]	1000 Sectors
13h	Host Read Commands	02h	16	[79:64]	count
14h	Host Write Commands	02h	16	[95:80]	count
15h	Controller Busy Time	02h	16	[111:96]	mins
16h	Power Cycles	02h	16	[127:112]	count
17h	Power on Hours	02h	16	[143:128]	hours
18h	Unsafe Shutdowns	02h	16	[159:144]	count
19h	Media and Data Integrity Errors	02h	16	[175:160]	times
1Ah	Number of Error Information Log Entries	02h	16	[191:176]	count
1Bh	Warning Composite Temperature Time	02h	4	[195:192]	mins
1Ch	Critical Composite Temperature Time	02h	4	[199:196]	mins
1Dh	Temperature Sensor 1	02h	2	[201:200]	°K
1Eh	Temperature Sensor 2	02h	2	[203:202]	°K
1Fh	Temperature Sensor 3	02h	2	[205:204]	°K
20h	Temperature Sensor 4	02h	2	[207:206]	°K
21h	Temperature Sensor 5	02h	2	[209:208]	°K
22h	Temperature Sensor 6	02h	2	[211:210]	°K
23h	Temperature Sensor 7	02h	2	[213:212]	°K
24h	Temperature Sensor 8	02h	2	[215:214]	°K
25h	Thermal Management Temperature 1 Transition Count	02h	4	[219:216]	count
26h	Thermal Management Temperature 2 Transition Count	02h	4	[223:220]	count
27h	Total Time for Thermal Management Temperature 1:	02h	4	[227:224]	Second
28h	Total Time for Thermal Management Temperature 2:	02h	4	[231:228]	Second
29h-4Fh	Reserved	02h		[511:232]	
50h	Flash Read Sector	C0h	8	[7:0]	sector
51h	Flash Write Sector	C0h	8	[15:8]	sector
52h	UNC Error	C0h	8	[23:16]	count
53h	PHY Error	C0h	4	[27:24]	count
54h	Early Bad Block	C0h	4	[31:28]	count
55h	Later Bad Block	C0h	4	[35:32]	count

56h	Max Erase Count	C0h	4	[39:36]	count
57h	Average Erase Count	C0h	4	[43:40]	count
58h	Current Percent Spares	C0h	8	[51:44]	%
59h	Current Temperature	C0h	2	[53:52]	°K
5Ah	Lowest Temperature	C0h	2	[55:54]	°K
5Bh	Highest Temperature	C0h	2	[57:56]	°K
5Ch	Current Controller Temperature	C0h	2	[61:60]	°K
5Dh	Spare Blocks	C0h	2	[63:62]	count

9. System Power Consumption

■ Supply Voltage

Parameter	Rating
Voltage	3.3V ± 5%
Current	1.6A

■ Power Consumption

SQF-C3M (DEFC)

(mW)		Read	Write	Idle
3D TLC (BiCS5)	256 GB	4,200	2,900	1,500
	512 GB	5,200	3,800	1,500

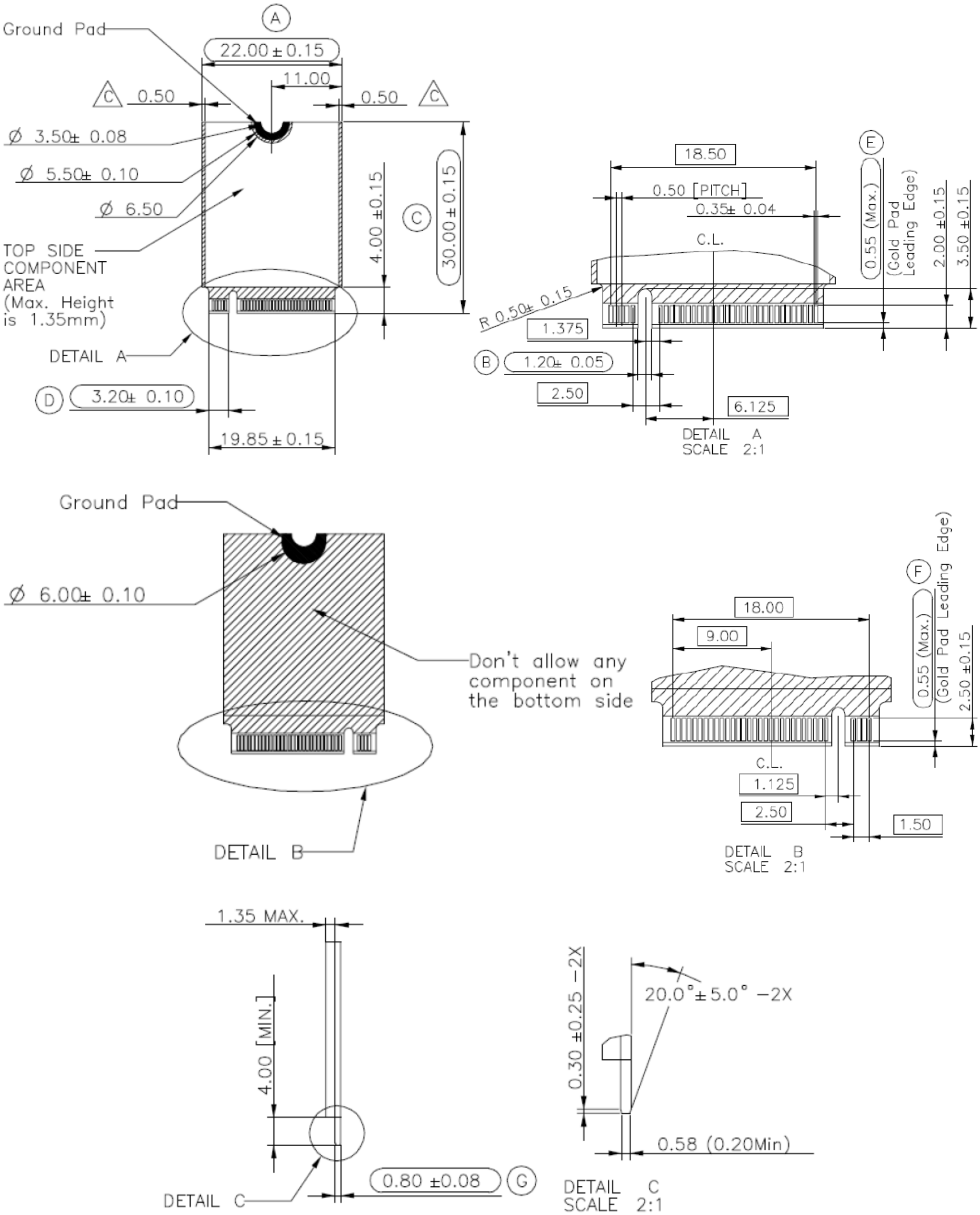
SQF-C3M (DEFE)

(mW)		Read	Write	Idle
3D TLC (BiCS5)	256 GB	3,400	2,500	1,500
	512 GB	3,800	3,200	1,500

1. Idle power consumption is measured at idle state with no write/read operation.
2. The measured power voltage of M.2 SSD is 3.3V.
3. Measurement environment: Room temperature: 20~25℃, humidity: 40~60%RH, DC+3.3V condition.
4. For SQF 730-D Embedded (Industrial) series SSD, it will not enter LPM (Low Power Mode) to avoid complex compatibility issues.
5. Power consumption may differ according to flash configuration, use condition, environment and platform configuration.

10. Physical Dimension

M.2 2230 (M key) PCIe/NVMe SSD (Unit: mm)



Appendix: Part Number Table

3D TLC (BiCS5)

Product	Advantech PN
SQF 730-D PCIe/NVMe M.2 2230 (M Key) 256G 3D TLC BiCS5 (0~70°C)	SQF-C3MV1-256GDEFC
SQF 730-D PCIe/NVMe M.2 2230 (M Key) 512G 3D TLC BiCS5 (0~70°C)	SQF-C3MV1-512GDEFC
SQF 730-D PCIe/NVMe M.2 2230 (M Key) 256G 3D TLC BiCS5 (-40~85°C)	SQF-C3MV1-256GDEFE
SQF 730-D PCIe/NVMe M.2 2230 (M Key) 512G 3D TLC BiCS5 (-40~85°C)	SQF-C3MV1-512GDEFE