mSATA 820 Datasheet

(SQF-SMSXX-XG-S8X)

CONTENTS

Revision History

Rev.	Date	History
0.1	2012/7/14	1. 1st draft
0.2	2013/2/14	1. Add Ultra MLC information 2. Update power consumption information
0.3	2013/3/15	1. Remove 40G/80G/160G wide temp. due to the absence of specific IC
0.4	2013/5/2	1. Separate performance information by Flash IC type
0.5	2013/6/2	1. Add 8GB MLC
1.0	2013/11/20	1. Add detail performance / TBW information 2. SLC upgrade to toggle SLC for SATA III performance, capacity up to 128GB
1.1	2013/12/13	1. Update power consumption information
1.2	2014/2/14	1. Add ext. temp. 256G MLC / 128G Ultra MLC
1.3	2014/3/14	1. Update TBW for latest Ultra MLC
1.4	2014/3/19	1. Update power consumption of 128G SLC
1.5	2014/6/9	1. Add 8G Ultra MLC information

1. Overview

Advantech SQFlash 820 series mSATA delivers all the advantages of Flash Disk technology with the Serial ATA III (6.0Gb) interface, fully compliant with standard mSATA form factor. The SQF-SMS is based on the mSATA form factor which is generated by JEDEC, designed to operate at a maximum operating frequency of 150MHz with 30MHz external crystal. Its capacity could provide a wide range from 4GB to 64GB for SLC, and 16GB to up to 256GB for MLC. Also it can reach more than 500MB/s read as well as 150MB/s write high performance even based on MLC flash. The power consumption of Flash Disk is also much lower than traditional Hard Drive.

2. Features

- **Standard SATA interface**
  - Support SATA 1.5/3.0/6.0 Gbps interface
  - SATA Revision 3.0 compliant
- **Operating Voltage：3.3V**
- **Support 72 bit ECC correct per 1K Byte data**
- **TRIM、AHCI supported**
- **AES256 and Hardware Quick Erase supported**
- **Temperature Ranges**
  - Commercial Temperature
    - 0℃ to 70℃ for operating
    - -40℃ to 85℃ for storage
  - Industrial Temperature
    - -40℃ to 85℃ for operating
    - -40℃ to 85℃ for storage
- **Mechanical Specification**
  - Shock：1,500G / 0.5ms
  - Vibration：20G / 80~2,000Hz
- **Humidty**
  - Humidity：5% ~ 95% under 55℃
- **Endurance : > 2,000,000 program/erase cycles**
  - This is a test result of the whole SQFlash drive. The test is to keep writing a fixed logical block address (LBA) and see if any bad blocks occur after 2M cycles. With wear-levelling mechanism, although the disk was kept writing the same LBA but the physical block changes per block writing. So this test also proves that wear-leveling is really working, or the block would be wearout after its designated life cycles.
- **Data Retention**
  - 10 years
- **Acquired RoHS、WHQL、CE、FCC Certificate**
- **Acoustic：0 dB**
- **Dimension：50.8 mm x 30.0 mm x 4.2 mm**

3. Specification Table

■ Performance

		Sequential Performance (MB/sec)		Random Performance (IOPS @4K)	
		Read	Write	Read	Write
SLC	16 GB	526	149	46,251	40,576
	32 GB	476	305	38,016	48,956
	64 GB	528	415	38,323	52,992
	128 GB	525	412	38,142	52,329
Ultra MLC	8 GB	510	180	41,882	47,488
	16 GB	510	165	45,082	44,160
	32 GB	521	292	45,440	59,366
	64 GB	521	290	45,440	59,674
	128 GB	528	467	37,990	58,650
MLC	16 GB	510	54	43,546	13,604
	32 GB	515	56	44,698	14,090
	64 GB	521	104	45,722	27,213
	128 GB	522	102	45,466	26,061
	160 GB	514	463	42,470	60,621
	256 GB	520	386	37,837	57,523

* All performance above are tested with AHCI mode.

Endurance

According to JEDEC subcommittee JC-64.8, the actual endurance of flash storage can be presented by Terabyte Write (TBW), which is measured by NAND Flash physical endurance, Wear-leveling Efficiency (WLE) and Write Amplification Factor (WAF) of specific capacities with following formula.

TBW = [(NAND Flash Physical Endurance) x Capacity x WLE] / WAF

- **TBW of sequential writing**

	WLE	WAF	TBW		
			SLC	Ultra MLC	MLC
8 GB	0.9200	1.0140	700	170	19
16 GB	0.9300	1.0120	1430	355	40
32 GB	0.9300	1.0113	2870	715	80
64 GB	0.9700	1.0070	6020	1505	180
128 GB	0.9600	1.0058	11930	2980	350
160 GB	0.9400	1.0082	--	--	430
256 GB	0.9600	1.0053	--	--	710

- **TBW of random writing**

	WLE	WAF	TBW		
			SLC	Ultra MLC	MLC
8 GB	0.8024	1.0258	610	150	12
16 GB	0.8639	1.0147	1330	330	30
32 GB	0.9303	1.0698	2710	675	80
64 GB	0.9696	1.1111	5450	1360	160
128 GB	0.9589	1.0519	11390	2845	340
160 GB	0.9571	1.0393	--	--	430
256 GB	0.9795	1.0279	--	--	710

4. General Description

Advanced NAND Flash Controller

Advantech SQFlash 820 series mSATA includes Bad Block Management Algorithm, Wear Leveling Algorithm, Error Detection / Correction Code (EDC/ECC) Algorithm, Fragment Writing Technology, and GuaranteedFlush Technology.

Bad Block Management

Bad blocks are blocks that contain one or more invalid bits of which the reliability is not guaranteed. Bad blocks may be representing when flash is shipped and may developed during life time of the device.

Advantech SQFlash 820 series mSATA implement an efficient bad block management algorithm to detect the factory produced bad blocks and manages any bad blocks that may develop over the life time of the device. This process is completely transparent to the user, user will not aware of the existence of the bad blocks during operation.

Wear Leveling

NAND Type flash have individually erasable blocks, each of which can be put through a finite number of erase cycles before becoming unreliable. It means after certain cycles for any given block, errors can be occurred in a much higher rate compared with typical situation. Unfortunately, in the most of cases, the flash media will not been used evenly. For certain area, like file system, the data gets updated much frequently than other area. Flash media will rapidly wear out in place without any rotation.

Wear leveling attempts to work around these limitations by arranging data so that erasures and re-writes are distributed evenly across the full medium. In this way, no single sector prematurely fails due to a high concentration of program/erase cycles.

Advantech SQFlash 820 series mSATA provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. By implement both dynamic and static wear leveling algorithms, the life expectancy of the flash media can be improved significantly.

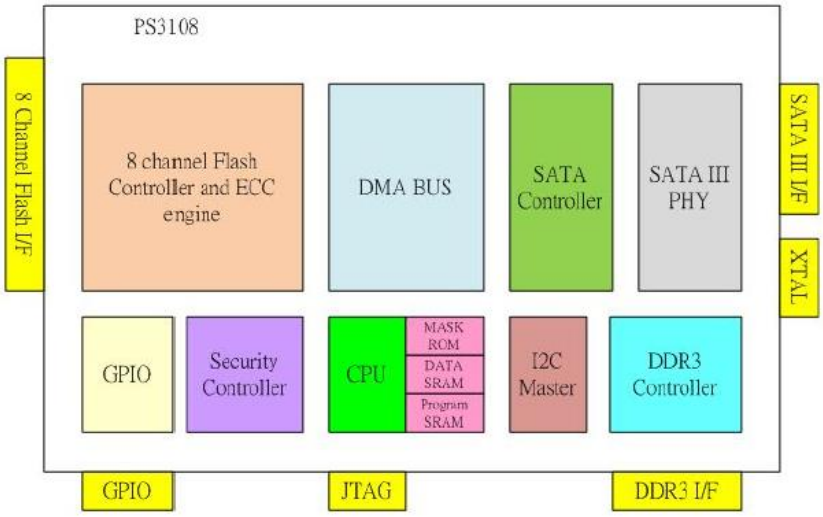
Error Detection / Correction

Advantech SQFlash 820 series mSATA utilizes BCH ECC Algorithm which offers one of the most powerful ECC algorithms in the industry. This algorithm can support 48/32/28 bit ECC correct per 2K Byte data.

Sophisticate Product Management Systems

Since industrial application require much more reliable devices compare with consumer product, a more sophisticated product management system become necessary for industrial customer requirement. The key to providing reliable devices is product traceability and failure analysis system. By implement such systems end customer can expect much more reliable product.

■ Block Diagram



■ LBA value

Density	LBA
4 GB	7,823,088
8 GB	15,649,200
16 GB	31,277,232
32 GB	62,533,296
64 GB	125,045,424
128 GB	250,069,680
160 GB	312,581,808
256 GB	500,118,192

5. Pin Assignment and Description

5.1 mSATA Interface Pin Assignments (Signal Segment)

Pin #	Function	Description
1	NC	No Connect
2	+3.3V	3.3V Source
3	NC	No Connect
4	DGND	Digital GND
5	NC	No Connect
6	NC	No Connect
7	NC	No Connect
8	NC	No Connect
9	DGND	Digital GND
10	NC	No Connect
11	NC	No Connect
12	NC	No Connect
13	NC	No Connect
14	NC	No Connect
15	DGND	Digital GND
16	NC	No Connect
17	NC	No Connect
18	DGND	Digital GND
19	NC	No Connect
20	NC	No Connect
21	SATA GND	SATA Ground Return Pin
22	NC	No Connect
23	TXP (out)	Host Receiver Differential Signal Pair
24	+3.3V	3.3V Source
25	TXN (out)	Host Receiver Differential Signal Pair
26	SATA GND	SATA Ground Return Pin
27	SATA GND	SATA Ground Return Pin
28	NC	No Connect
29	SATA GND	SATA Ground Return Pin
30	NC	No Connect
31	RXN (in)	Host Transmitter Differential Signal Pair
32	NC	No Connect
33	RXP (in)	Host Transmitter Differential Signal Pair
34	DGND	Digital GND
35	SATA GND	SATA Ground Return Pin
36	NC	No Connect
37	SATA GND	SATA Ground Return Pin
38	NC	No Connect
39	+3.3V	3.3V Source
40	DGND	Digital GND
41	+3.3V	3.3V Source
42	NC	No Connect
43	NC	No Coneect

44	NC	No Connect
45	NC	Reserved pin
46	NC	No Connect
47	NC	Reserved pin
48	NC	No Connect
49	DA/DSS (option)	Option for LED output
50	DGND	Digital GND
51	GND	Default connect to GND
52	+3.3V	3.3V Source

6. Identify Device Data

The Identity Device Data enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero

Word Address	F：Fixed V：Variable X：Both	Default Value	Data Field Type Information
0	F	0400h	General configuration bit-significant information
1	X	3FFFh	Obsolete – Number of logical cylinders (16383)
2	V	C837h	Specific configuration
3	X	0010h	Obsolete – Number of logical heads (16)
4-5	X	00000000h	Retired
6	X	003Fh	Obsolete – Number of logical sectors per logical track (63)
7-8	V	00000000h	Reserved for assignment by the Compact Flash Association
9	X	0000h	Retired
10-19	F	Varies	Serial number (20 ASCII characters)
20-21	X	0000h	Retired
22	X	0000h	Obsolete
23-26	F	Varies	Firmware revision (8 ASCII characters)
27-46	F	Varies	Model number (xxxxxxxx)
47	F	8010h	7:0- Maximum number of sectors transferred per interrupt on MULTIPLE commands
48	F	0000h	Reserved
49	F	2F00h	Capabilities
50	F	4000h	Capabilities
51-52	X	000000000h	Obsolete
53	F	0007h	Words 88 and 70:64 valid
54	X	3FFFh	Obsolete – Number of logical cylinders (16383)
55	X	0010h	Obsolete – Number of logical heads (16)
56	X	003Fh	Obsolete – Number of logical sectors per track (63)
57-58	X	00FBFC10h	Obsolete – Current capacity in sectors –
59	F	0110h	Number of sectors transferred per interrupt on MULTIPLE commands
60-61	F	4GB – 1TB	Total number of user addressable sectors
62	X	0000h	Obsolete
63	F	0407h	Multi-word DMA modes supported/selected
64	F	0003h	PIO modes supported
65	F	0078h	Minimum Multiword DMA transfer cycle time per word
66	F	0078h	Manufacturer’s recommended Multiword DMA transfer cycle time
67	F	0078h	Minimum PIO transfer cycle time without flow control

68	F	0078h	Minimum PIO transfer cycle time with IORDY flow control
69	F	0100h	Additional Supported (support download microcode DMA)
70	F	0000h	Reserved
71-74	F	0000000000000000h	Reserved for the IDENTIFY PACKET DEVICE command
75	F	001Fh	Queue depth
76	F	0706h	Serial SATA capabilities
77	F	0000h	Reserved for future Serial ATA definition
78	F	0044Ch	Serial ATA features supported
79	V	0040H	Serial ATA features enabled
80	F	01F8h	Major Version Number
81	F	0000h	Minor Version Number
82	F	346bh	Command set supported
83	F	70d9h	Command set supported
84	F	6023h	Command set/feature supported extension
85	V	3469h	Command set/feature enabled
86	V	bc01h	Command set/feature enabled
87	V	6023h	Command set/feature default
88	V	003Fh	Ultra DMA Modes
89	F	001Eh	Time required for security erase unit completion
90	F	001Eh	Time required for Enhanced security erase completion
91	V	0000h	Current advanced power management value
92	V	FFFEh	Master Password Revision Code
93	F	0000h	Hardware reset result. The contents of the bits (12:0) of this word shall change only during the execution of s hardware reset.
94	V	0000h	Vendor's recommended and actual acoustic management value
95	F	0000h	Stream Minimum Request Size
96	V	0000h	Streaming Transfer Time – DMA
97	V	0000h	Streaming Access Latency – DMA and PIO
98-99	F	0000h	Streaming Performance Granularity
100-103	V	4GB – 1TB	Maximum user LBA for 48 bit Address feature set
104	V	0000h	Streaming Transfer Time – PIO
105	F	0000h	Maximum number of 512-byte blocks per DATA SET MANAGEMENT command
106	F	4000h	Physical sector size / Logical sector size
107	F	0000h	Inter-seek delay for ISO-7779 acoustic testing in microseconds
108-111	F	0000000000000000h	Unique ID
112-115	F	0000000000000000h	Reserved

116	V	0000h	Reserved
117-118	F	00000000h	Words per logical Sector
119	F	4015h	Supported settings
120	F	4015h	Command set/Feature Enabled/Supported
121-126	F	0h	Reserved
127	F	0h	Removable Media Status Notification feature set support
128	V	0021h	Security status
129-159	X	0h	Vendor specific
160	F	0h	Compact Flash Association (CFA) power mode 1
161-167	X	0h	Reserved for assignment by the CFA
168	F	2.5 inch – 3h 1.8 inch – 4h Less than 1.8 inch – 5h	Device Nominal Form Factor
169	F	0001h	DATA SET MANAGEMENT command is supported
170-173	F	0h	Additional Product Identifier
174-175		0h	Reserve
176-205	V	0h	Current media serial number
206	F	0h	SCT Command Transport(
207-208	F	0h	Reserved
209	F	4000h	Alignment of logical blocks within a physical block
210-211	V	0000h	Write-Read-Verify Sector Count Mode 3 (not support)
212-213	F	0000h	Write-Read-Verify Sector Count Mode 2 (not support)
214-216		0000h	NV Cache relate (not support)
217	F	0001h	Non-rotating media device
218	F	0h	Reserved
219	F	0h	NV Cache relate (not support)
220	V	0h	Write read verify feature set current mode
221		0h	Reserved
222	F	101Fh	Transport major version number
223	F	0h	Transport minor version number
224-229		0h	Reserved
230-233		0h	Extend number of user addressable sectors
234		0001h	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
235		00FFh	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
236-254	F	0h	Reserved
255	X	XXA5h XX is variable	Integrity word (Checksum and Signature)

7. ATA Command Set

[Command Set List]

No.	Command set	Code	Protocol	Argument
1	CHECK POWER MODE	E5h	ND	28-bit
2	DOWNLOAD MICROCODE	92h	PO	28-bit
3	EXECUTE DEVICE DIAGNOSTIC	90h	DD	28-bit
4	FLUSH CACHE	E7h	ND	28-bit
5	FLUSH CACHE EXT	EAh	ND	28-bit
6	IDENTIFY DEVICE	ECh	PI	28-bit
7	IDLE	E3h	ND	28-bit
8	IDLE IMMEDIATE	E1h	ND	28-bit
9	INITIALIZE DEVICE PARAMETERS	91h	ND	28-bit
10	NOP	00h	ND	28-bit
11	READ BUFFER	E4h	PI	28-bit
12	READ DMA	C8h,C9h	DM	28-bit
13	READ DMA EXT	25h	DM	48-bit
14	READ MULTIPLE	C4h	PI	28-bit
15	READ MULTIPLE EXT	29h	PI	48-bit
16	READ NATIVE MAX ADDRESS	F8h	ND	28-bit
17	READ NATIVE MAX ADDRESS EXT	27h	ND	48-bit
18	READ SECTOR(S)	20h,21h	PI	28-bit
19	READ SECTOR(S) EXT	24h	PI	48-bit
20	READ VERIFY SECTOR(S)	40h,41h	ND	28-bit
21	READ VERIFY EXT	42h	ND	48-bit
22	RECALIBRATE	1Xh	ND	28-bit
23	SECURITY DISABLE PASSWORD	F6h	PO	28-bit
24	SECURITY ERASE PREPARE	F3h	ND	28-bit
25	SECURITY ERASE UNIT	F4h	PO	28-bit
26	SECURITY FREEZE	F5h	ND	28-bit
27	SECURITY SET PASSWORD	F1h	PO	28-bit
28	SECURITY UNLOCK	F2h	PO	28-bit
29	SEEK	7Xh	ND	28-bit
30	SET MAX ADDRESS	F9h	ND	28-bit
31	SET MAX ADDRESS EXT	37h	ND	48-bit
32	SET FEATURE	EFh	ND	28-bit
33	SET MULTIPLE	C6h	ND	28-bit
34	SLEEP	E6h	ND	28-bit
35	SMART READ DATA	B0h		
36	SMART ENABLE/DISABLE AUTO SAVE	B0h		
37	SMART EXECUTE OFF-LINE	B0h		
38	SMART READ LOG	B0h		
39	SMART ENABLE OPERATION	B0h		
40	SMART DISABLE OPERATION	B0h		
41	SMART RETURN STATUS	B0h		
42	STANDBY	E2h	ND	28-bit
43	STANDBY IMMEDIATE	E0h	ND	28-bit
44	WRITE BUFFER	E8h	PO	28-bit
45	WRITE DMA	CAh,CBh	DM	28-bit
46	WRITE DMA EXT	35h	DM	48-bit
47	WRITE MULTIPLE	C5h	PO	28-bit
48	WRITE MULTIPLE EXT	39h	PO	48-bit

49	WRITE SECTOR(S)	30h	PO	28-bit
50	WRITE SECTOR(S) EXT	34h	PO	48-bit
51	WRITE SECTOR(S) W/O ERASE	38h	PO	28-bit
52	WRITE VERIFY	3Ch	PO	28-bit

Note: ND = Non-Data Command
PI = PIO Data-In Command
PO = PIO Data-Out Command
DM = DMA Command
DD = Execute Diagnostic Command

[Command Set Descriptions]

1. CHECK POWER MODE (code: E5h);
This command allow host to determine the current power mode of the device.

2. DOWNLOAD MICROCODE (code: 92h);
This command enable the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE command is vendor specific.
All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the content of the LBA Low register and the Sector Count register.
This allows transfer sizes from 0 bytes to 33,553,920 bytes, in 512bytes increments.

3. EXECUTE DEVICE DIAGNOSTIC (code: 90h);
This command performs the internal diagnostic tests implemented by the module.

4. FLUSH CACHE (code: E7h);
This command used by the host to request the device to flush the write cache.

5. FLUSH CACHE EXT (code: EAh);
This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media.

6. IDENTIFY DEVICE (code: ECh);
The IDENTIFY DEVICE command enables the host to receive parameter information from the module.

7. IDLE (code: 97h or E3h);
This command allows the host to place the module in the IDLE mode and also set the Standby timer. INTRQ may be asserted even through the module may not have fully transitioned to IDLE mode. If the Sector Count register is non-"0", then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer. If the Sector Count register is "0" then the Standby timer is disabled.

8. IDLE IMMEDIATE (code: E1h);
This command causes the module to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.

9. INITIALIZE DEVICE PARAMETERS (code: 91h);
This command enables the host to set the number of sectors per track and the number of heads per cylinder.

10. NOP (code: 00h);
If this command is issued, the module respond with command aborted.

11. READ BUFFER (code: E4h);

This command enables the host to read the current contents of the module's sector buffer.

12. READ DMA (code: C8h or C9h);

This command reads from “1” to “256” sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of “0” requests “256” sectors transfer. The transfer begins at the sector specified in the Sector Number register.

13. READ DMA Ext (code: 25h);

This command allows the host to read data using the DMA data transfer protocol.

14. READ MULTIPLE (code: C4h);

This command performs similarly to the READ SECTORS command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sector per block is defined by the content of word 59 in the IDENTIFY DEVICE response.

15. READ MULTIPLE EXT (code: 29h);

This command performs similarly to the READ SECTORS command. The number of sectors per block is defined by a successful SET MULTIPLE command. If no successful SET MULTIPLE command has been issued, the block is defined by the device’s default value for number of sectors per block as defined in bits (7:0) in word 47 in the IDENTIFY DEVICE information.

16. READ NATIVE MAX ADDRESS (code: F8h);

This command returns the native maximum address. The native maximum address is the highest address accepted by the device in the factory default condition.

17. READ NATIVE MAX ADDRESS EXT (code: 27h);

This command returns the native maximum address.

18. READ SECTOR(S) (code: 20h or 21h);

This command reads from “1” to “256” sectors as specified in the Sector Count register. A sector count of “0” requests “256” sectors transfer. The transfer begins at the sector specified in the Sector Number register.

19. READ SECTOR(S) EXT (code: 24h);

This command reads from “1” to “65536” sectors as specified in the Sector Count register. A sector count of “0” requests “65536” sectors transfer. The transfer begins at the sector specified in the Sector Number register.

20. READ VERIFY SECTOR(S) (code: 40h or 41h);

This command is identical to the READ SECTORS command, except that DRQ is never set and no data is transferred to the host.

21. READ VERIFY SECTOR(S) EXT (code: 42h);

This command is identical to the READ SECTORS command, except that DRQ is never set and no data is transferred to the host.

22. RECALIBRATE (code: 1Xh);

This command return value is select address mode by the host request.

23. SECURITY DISABLE PASSWORD (code: F6h);

This command transfers 512 bytes of data from the host. Table defines the content of this information. If the password selected by word 0 match the password previously saved by the device, the device shall disable the Lock mode. This command shall not change the Master password. The Master password shall be reactivated when a User password is set.

24. SECURITY ERASE PREPARE (code: F3h);

This command shall be issued immediately before the SECURITY ERASE UNIT command to enable device eraseing and unlocking.

25. SECURITY ERASE UNIT (code: F4h);

This command transfer 512 bytes of data from the host. Table## defines the content of this information. If the password does not match the password previously saved by the device, the device shall reject the command with command aborted.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command.

26. SECURITY FREEZE LOCK (code: F5h);

This command shall set the device to frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen shall be disabled by power-off or hardware reset.

If SECURITY FREEZE LOCK is issued when the drive is in frozen mode, the drive executes the command and remains in frozen mode.

27. SECURITY SET PASSWORD (code: F1h);

This command transfer 512 bytes of data from the host. Table defines the content of this information. The data transferred controls the function of this command. Table defines the interaction of the identifier and security level bits.

28. SECURITY UNLOCK (code: F2h);

This command transfer 512 bytes of data from the host. Table (as Disable Password) defines the content of this information.

If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the identifier bit is set to user then the device shall compare the supplied password with the stored User password.

If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall be decremented for each password mismatch when SECURITY UNLOCK is issued and the device is locked. When this counter reachs zero then SECURITY UNLOCK and SECURITY ERASE UNIT command shall be aborted unitl a power-on or a hardware reset.

29. SEEK (code: 7Xh);

This command performs address range check.

30. SET MAX ADDRESS (code: F9h);

After successful command completion, all read and write access attempts to address greater than specified by the successful SET MAX ADDRESS command shall be rejected with an IDNF error. IDENTIFY DEVICE response words (61:60) shall reflect the maximum address set with this command.

31. SET MAX ADDRESS EXT (code: 37h);

After successful command completion, all read and write access attempts to address greater than specified by the successful SET MAX ADDRESS command shall be rejected with an IDNF error. IDENTIFY DEVICE response words (61:60) shall reflect the maximum address set with this command.

32. SET FEATURE (code: EFh);

This command is used by the host to establish parameters that affect the execution of certain device features.

33. SET MULTIPLE MODE (code: C6h);
This command enables the device to perform READ and Write Multiple operations and establishes the block count for these commands.

34. SLEEP (code: 99h or E6h);
This command causes the module to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

35. SMART READ DATA (code: B0h with Feature register value of D0h);
This command returns the Device SMART data structure to the host.

36. SMART ENABLE/DISABLE AUTO SAVE (code: B0h with Feature register value of D2h);
This command enables and disables the optional attribute autosave feature of the device.

37. SMART EXECUTE OFF_LINE (code: B0h with Feature register value of D4h);
This command cause the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile memory, or execute a self-diagnostic test routine in either captive or off-line mode.

38. SMART READ LOG (code: B0h with Feature register value of D5h);
This command returns the specified log data to the host.

39. SMART ENABLE OPERATION (code: B0h with Feature register value of D8h);
This command enables access to all SMART capabilities within the device. Prior to receipt of this command SMART data are neither monitored nor saved by the device.

40. SMART DISABLE OPERATION (code: B0h with Feature register value of D9h);
This command disables all SMART capabilities within the device including any and all timer and event count functions related exclusively to this feature. After command acceptance the device shall disable all SMART operations.
After receipt of this command by the device, all other SMART commands including SMART DISABLE OPERATION commands, with exception of SMART ENABLE OPERATIONS, are disabled and invalid and shall be command aborted by the device.

41. SMART RETURN STATUS (code: B0h with Feature register value of DAh);
This command cause the device to communicate the reliability status of the device to the host.

42. STANDBY (code: E2h);
This command causes the module to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.

43. STANDBY IMMEDIATE (code: E0h);
This command causes the module to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.

44. WRITE BUFFER (code: E8h);
This command enables the host to overwrite contents of the module's sector buffer with any data pattern desired.

45. WRITR DMA (code: CAh or CBh);
This command writes from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

46. WRITR DMA EXT (code: 35h);

This command writes from “1” to “65536” sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of “0” requests “65536” sectors transfer. The transfer begins at the sector specified in the Sector Number register.

47. WRITE MULTIPLE (code: C5h);

This command is similar to the WRITE SECTORS command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

48. WRITE MULTIPLE EXT (code: 39h);

This command is similar to the WRITE SECTORS command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

49. WRITE SECTOR(S) (code: 30h);

This command writes from “1” to “256” sectors as specified in the Sector Count register. A sector count of “0” requests “256” sectors transfer. The transfer begins at the sector specified in the Sector Number register.

50. WRITE SECTOR(S) EXT (code: 34h);

This command writes from “1” to “65536” sectors as specified in the Sector Count register. A sector count of “0” requests “65536” sectors transfer. The transfer begins at the sector specified in the Sector Number register.

51. WRITE SECTOR(S) W/O ERASE (code: 38h);

This command writes from “1” to “256” sectors as specified in the Sector Count register. A sector count of “0” requests “256” sectors transfer. The transfer begins at the sector specified in the Sector Number register.

52. WRITE VERIFY (code: 3Ch);

This command is similar to the WRITE SECTOR(S) command, except that each sector is verified before the command is completed.

8. System Power Consumption

8.1 Supply Voltage

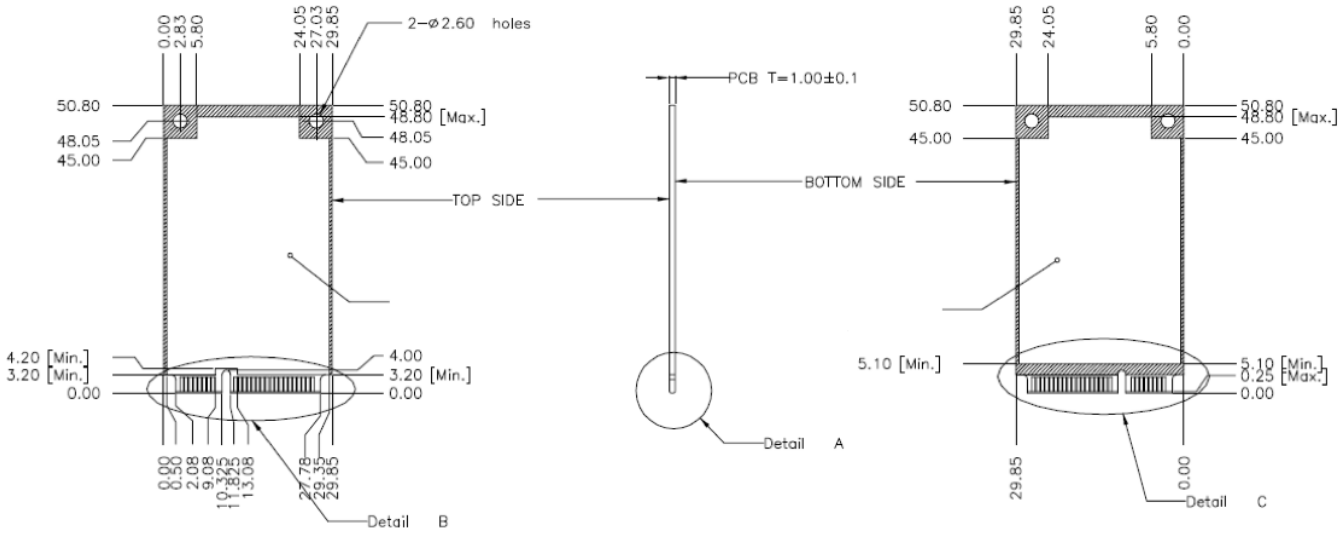
Parameter	Rating
Operating Voltage	3.3V

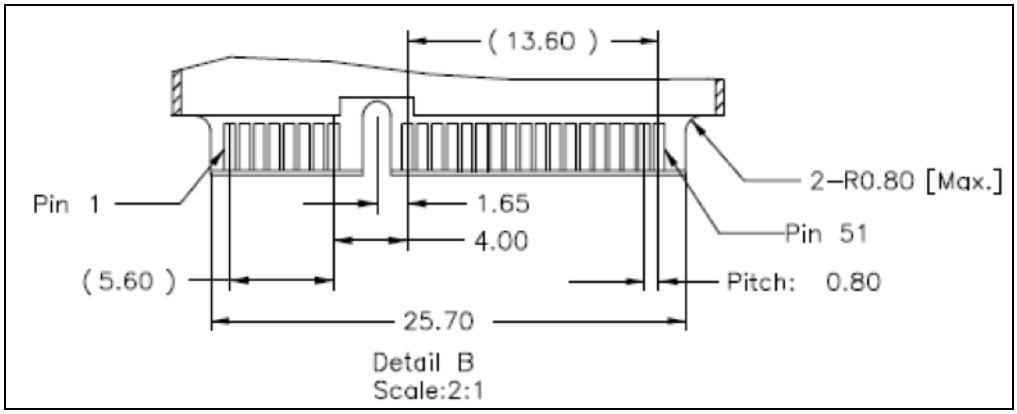
8.2 Power Consumption

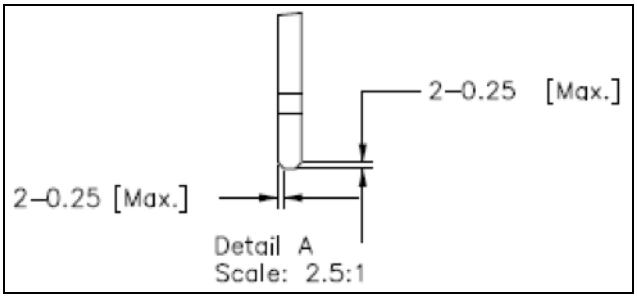
mA		Read	Write	Idle	Slumber
SLC	16 GB	680	470	66	15
	32 GB	590	620	66	15
	64 GB	660	710	66	15
	128 GB	845	940	86	18
Ultra MLC	16 GB	580	510	61	13
	32 GB	560	730	60	10
	64 GB	615	780	55	22
	128 GB	830	850	94	23
MLC	16 GB	570	340	69	17
	32 GB	555	350	48	17
	64 GB	555	440	64	11
	128 GB	610	480	70	18
	160 GB	660	970	72	19
	256 GB	680	860	74	22

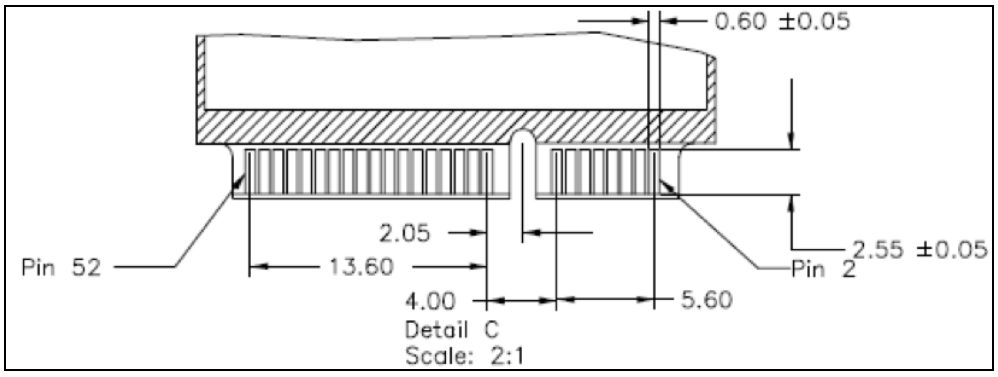
9. Physical Dimension

mSATA SSD (Unit: mm)









Appendix: Part Number Table

Product	Advantech PN
SQF MSATA 820 8G SLC 2-CH (0~70°C)	SQF-SMSS2-8G-S8C
SQF MSATA 820 16G SLC 4-CH (0~70°C)	SQF-SMSS4-16G-S8C
SQF MSATA 820 32G SLC 4-CH (0~70°C)	SQF-SMSS4-32G-S8C
SQF MSATA 820 64G SLC 4-CH (0~70°C)	SQF-SMSS4-64G-S8C
SQF MSATA 820 128G SLC 4-CH (0~70°C)	SQF-SMSS4-128G-S8C
SQF MSATA 820 8G SLC 2-CH (-40~85°C)	SQF-SMSS2-8G-S8E
SQF MSATA 820 16G SLC 4-CH (-40~85°C)	SQF-SMSS4-16G-S8E
SQF MSATA 820 32G SLC 4-CH (-40~85°C)	SQF-SMSS4-32G-S8E
SQF MSATA 820 64G SLC 4-CH (-40~85°C)	SQF-SMSS4-64G-S8E
SQF MSATA 820 128G SLC 4-CH (-40~85°C)	SQF-SMSS4-128G-S8E
SQF MSATA 820 8G UMLC 4-CH (0~70°C)	SQF-SMSU4-8G-S8C
SQF MSATA 820 16G UMLC 4-CH (0~70°C)	SQF-SMSU4-16G-S8C
SQF MSATA 820 32G UMLC 4-CH (0~70°C)	SQF-SMSU4-32G-S8C
SQF MSATA 820 64G UMLC 4-CH (0~70°C)	SQF-SMSU4-64G-S8C
SQF MSATA 820 128G UMLC 4-CH (0~70°C)	SQF-SMSU4-128G-S8C
SQF MSATA 820 8G UMLC 4-CH (-40~85°C)	SQF-SMSU4-8G-S8E
SQF MSATA 820 16G UMLC 4-CH (-40~85°C)	SQF-SMSU4-16G-S8E
SQF MSATA 820 32G UMLC 4-CH (-40~85°C)	SQF-SMSU4-32G-S8E
SQF MSATA 820 64G UMLC 4-CH (-40~85°C)	SQF-SMSU4-64G-S8E
SQF MSATA 820 128G UMLC 4-CH (-40~85°C)	SQF-SMSU4-128G-S8E
SQF MSATA 820 8G MLC 2-CH (0~70°C)	SQF-SMSM2-8G-S8C
SQF MSATA 820 16G MLC 4-CH (0~70°C)	SQF-SMSM4-16G-S8C
SQF MSATA 820 32G MLC 4-CH (0~70°C)	SQF-SMSM4-32G-S8C
SQF MSATA 820 64G MLC 4-CH (0~70°C)	SQF-SMSM4-64G-S8C
SQF MSATA 820 128G MLC 4-CH (0~70°C)	SQF-SMSM4-128G-S8C
SQF MSATA 820 160G MLC 5-CH (0~70°C)	SQF-SMSM5-160G-S8C
SQF MSATA 820 256G MLC 8-CH (0~70°C)	SQF-SMSM8-256G-S8C
SQF MSATA 820 8G MLC 2-CH (-40~85°C)	SQF-SMSM2-8G-S8E
SQF MSATA 820 16G MLC 4-CH (-40~85°C)	SQF-SMSM4-16G-S8E
SQF MSATA 820 32G MLC 4-CH (-40~85°C)	SQF-SMSM4-32G-S8E
SQF MSATA 820 64G MLC 4-CH (-40~85°C)	SQF-SMSM4-64G-S8E
SQF MSATA 820 128G MLC 4-CH (-40~85°C)	SQF-SMSM4-128G-S8E
SQF MSATA 820 256G MLC 8-CH (-40~85°C)	SQF-SMSM8-256G-S8E